

Datasheet

G32A1085

G32A1065

G32A1045

**Arm[®] Cortex[®]-M0+ based 32-bit
Automotive-grade MCU**

Version: V1.2

1 Product Characteristics

■ Core

- 32-bit Arm® Cortex®-M0+ core with MPU
- Up to 64MHz working frequency

■ Memory

- Up to 256KB PFlash with ECC
- Up to 32KB DFlash with ECC
- Up to 32KB SRAM with ECC

■ Clock

- HSECLK: External 8~20MHz crystal oscillator
- HSICLK: Internal 8MHz RC oscillator
- HSICLK14: Internal 14MHz RC oscillator
- LSICLK: Internal 32kHz RC oscillator
- PLL supports 2~16 times frequency

■ Reset and power management

- Power On/Power Off Reset (POR/PDR)

- Digital supply voltage:

$$V_{DD}=2.75\sim 5.5V$$

- Analog supply voltage:

$$V_{DDA}=V_{DD}\sim 5.5V$$

- Support programmable voltage detector PVD

■ Low-power mode

- Stop mode, Sleep mode, Standby mode
- Support CAN、USART(LIN)、I/O、RTC、IWDG wakeup

■ DMA

- One 5-channel DMA controller

■ Serial wire debug (SWD)

■ I/O

- Up to 55 I/O
- All I/O can be mapped to external interrupt vector

■ Communication peripherals

- 2 USART interfaces, all support master synchronous mode and modem control, both support LIN,

automatic baud rate detection and wake-up, maximum rate 8Mbit/s

- 1 SPI interface (16Mbit/s)
- 1 CAN interface, support CAN2.0A/B and CAN FD protocol (ISO 11898-1)

■ Analog peripherals

- 1 12-bit ADC, supporting up to 16 external and 3 internal channels

■ Timer

- 1 16-bit advanced timer TMR1 with up to 7 channels of PWM output, supporting deadband generation and brake input
- 3 16-bit general timers TMR2/3/4, each with up to 4 independent channels for input capture, output comparison, PWM and pulse counting functions
- 3 16-bit basic timers TMR6/7/8
- 1 independent watchdog IWDT, supporting window mode
- 1 system tick timer
- 1 RTC timer

■ Information security

- CRC computing unit
- AES256 cryptographic module
- SHA256 Hash function
- TRNG generator
- 96-bit unique ID

■ Package

- LQFP64
- LQFP48
- QFN32 (4mm x 4mm)

■ Operating temperature

- Range: -40°C ~125°C

■ Certification

- AEC-Q100 Grade1
- ISO 26262 ASIL-B

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2 Product Information

See the table for G32A1085 A1065 A1045 product functions and peripheral configurations.

Table 1 Functions and Peripherals of G32A1085 A1065 A1045 Series Chips

Product		G32A1085			G32A1065			G32A1045	
Model		MAT0MFM	MAT0MLF	MAT0MLH	MAT0MFM	MAT0MLF	MAT0MLH	MAT0MFM	MAT0MLF
Package		QFN32	LQFP48	LQFP64	QFN32	LQFP48	LQFP64	QFN32	LQFP48
Core and maximum working frequency		Arm® Cortex®-M0+ 32-bit @64MHz							
Working voltage		2.75V~5.5V							
PFlash(KB) with ECC		256			128			64	
DFlash(KB) with ECC		32						16	
SRAM(KB) with ECC		32			16			8	
GPIO		26	39	55	26	39	55	26	39
Communication interface	USART	2							
	SPI	1							
	CAN (CAN FD)	1							
Timer	16-bit advanced	1							
	16-bit general	3							
	16-bit basic	3							
	SysTick timer	1							

Product		G32A1085			G32A1065			G32A1045	
Model		MAT0MFM	MAT0MLF	MAT0MLH	MAT0MFM	MAT0MLF	MAT0MLH	MAT0MFM	MAT0MLF
Package		QFN32	LQFP48	LQFP64	QFN32	LQFP48	LQFP64	QFN32	LQFP48
	RTC	1							
	Watchdog (With window mode)	1							
12-bit ADC	Unit	1							
	External channels	10		16	10		16	10	
	Internal channels	3							
TRNG		1							
AES256		1							
SHA256		1							
Operating temperature		Ambient temperature: -40°C to 125°C							

3 Pin Information

3.1 Pin distribution

Figure 1 Distribution Diagram of G32A1085 A1065 Series LQFP64 Pins

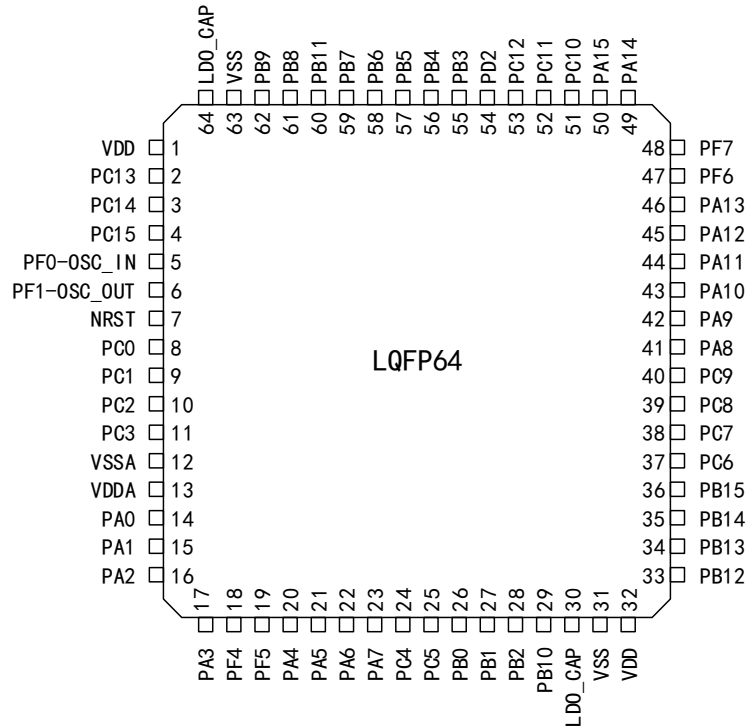


Figure 2 Distribution Diagram of G32A1085 A1065 A1045 Series LQFP48 Pins

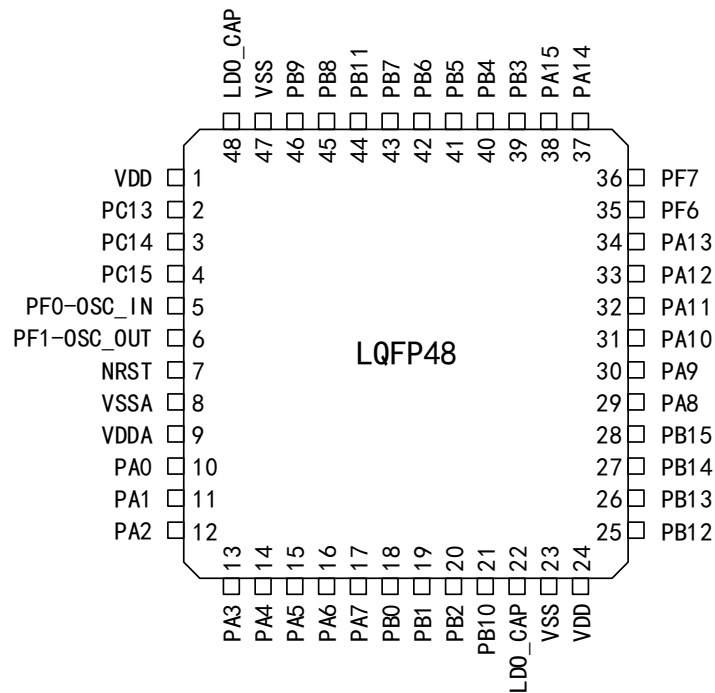
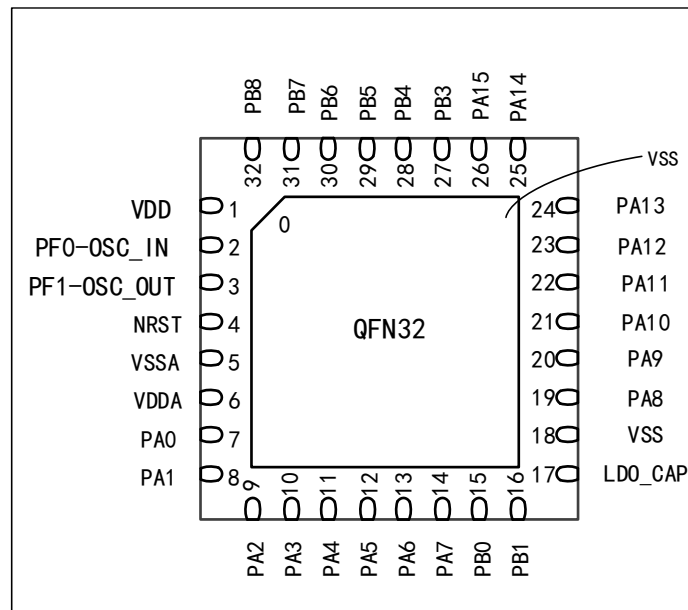


Figure 3 Distribution Diagram of G32A1085 A1065 A1045 Series QFN32 Pins



3.2 Pin function description

Table 2 Legends/Abbreviations Used in Output Pin Table

Name	Abbreviation	Definition
Pin name		Unless otherwise specified in parentheses below the pin name, the pin functions during and after reset are the same as the actual pin name
Pin type	P	Power pin
	I	Only input pin
	I/O	I/O pin
I/O structure	STD	Standard I/O
	STDA	Directly connected to ADC I/O
	RST	Bidirectional reset pin with built-in weak pull-up resistor
Notes		Unless otherwise specified, all I/O pins are set as floating input during and after reset
Pin function	Multiplexing functions	Functions selected via GPIOx_AFR registers
	Additional functions	Functions directly selected/enabled via peripheral registers

Table 3 G32A1085 A1065 A1045 Functional Description

Name (Function after reset)	Type	I/O	Default multiplexing function	Additional function	QFN32	LQFP48	LQFP64
VDD	P	-	VDD	VDD	1	1	1

Name (Function after reset)	Type	I/O	Default multiplexing function	Additional function	QFN32	LQFP48	LQFP64
PC13	I/O	STD	TMR1_CH1	-	-	2	2
PC14	I/O	STD	TMR1_CH2	-	-	3	3
PC15	I/O	STD	TMR1_CH3	-	-	4	4
PF0- OSC_IN (PF0)	I/O	STD	-	OSC_IN	2	5	5
PF1- OSC_OUT (PF1)	I/O	STD	-	OSC_OUT	3	6	6
NRST	I/O	RST	System reset input/ Internal reset output	NRST	4	7	7
PC0	I/O	STDA	EVENTOUT, USART2_TX	ADC_IN10	-	-	8
PC1	I/O	STDA	EVENTOUT, USART2_RX	ADC_IN11	-	-	9
PC2	I/O	STDA	EVENTOUT	ADC_IN12	-	-	10
PC3	I/O	STDA	EVENTOUT	ADC_IN13	-	-	11
VSSA	P	-	VSSA	VSSA	5	8	12
VDDA	P	-	VDDA	VDDA	6	9	13
PA0	I/O	STDA	USART2_CTS, TMR2_CH1, CAN_RX	ADC_IN0	7	10	14
PA1	I/O	STDA	USART2_RTS, EVENTOUT, TMR2_CH2, CAN_TX, TMR4_CH2	ADC_IN1	8	11	15
PA2	I/O	STDA	TMR4_CH1, USART2_TX, TMR2_CH3	ADC_IN2	9	12	16
PA3	I/O	STDA	TMR4_CH2, USART2_RX, TMR2_CH4	ADC_IN3	10	13	17
PF4	I/O	STD	EVENTOUT	-	-	-	18
PF5	I/O	STD	EVENTOUT	-	-	-	19
PA4	I/O	STDA	SPI1_NSS, USART2_CK, TMR4_CH1	ADC_IN4	11	14	20
PA5	I/O	STDA	SPI1_SCK, TMR2_CH1	ADC_IN5	12	15	21

Name (Function after reset)	Type	I/O	Default multiplexing function	Additional function	QFN32	LQFP48	LQFP64
PA6	I/O	STDA	SPI1_MISO, TMR3_CH1, TMR1_BKIN, CAN_RX, TMR4_CH3, EVENTOUT	ADC_IN6	13	16	22
PA7	I/O	STDA	SPI1_MOSI, TMR3_CH2, TMR1_CH1N, CAN_TX, TMR4_CH4, EVENTOUT	ADC_IN7	14	17	23
PC4	I/O	STDA	EVENTOUT	ADC_IN14	-	-	24
PC5	I/O	STDA	TMR1_CH4	ADC_IN15	-	-	25
PB0	I/O	STDA	USART1_TX, TMR3_CH3, TMR1_CH2N	ADC_IN8	15	18	26
PB1	I/O	STDA	USART1_RX, TMR3_CH4, TMR1_CH3N	ADC_IN9	16	19	27
PB2	I/O	STD	TMR1_CH1N	-	-	20	28
PB10	I/O	STD	TMR2_CH3, EVENTOUT	-	-	21	29
LDO_CAP	P	-	LDO_CAP	LDO_CAP	17	22	30
VSS	P	-	VSS	VSS	18	23	31
VDD	P	-	VDD	VDD	-	24	32
PB12	I/O	STD	TMR1_BKIN, EVENTOUT	-	-	25	33
PB13	I/O	STD	TMR1_CH1N, TMR2_CH4	-	-	26	34
PB14	I/O	STD	TMR4_CH1, TMR1_CH2N	-	-	27	35
PB15	I/O	STD	TMR4_CH2, TMR1_CH3N, TMR2_CH3	-	-	28	36
PC6	I/O	STD	TMR3_CH1	-	-	-	37
PC7	I/O	STD	TMR3_CH2	-	-	-	38
PC8	I/O	STD	TMR3_CH3	-	-	-	39
PC9	I/O	STD	TMR3_CH4	-	-	-	40
PA8	I/O	STD	USART1_CK, TMR1_CH1, EVENTOUT, MCO	-	19	29	41
PA9	I/O	STD	TMR4_CH3, USART1_TX, TMR1_CH2	-	20	30	42
PA10	I/O	STD	USART1_RX, TMR1_CH3	-	21	31	43
PA11	I/O	STD	USART1_CTS, TMR1_CH4, EVENTOUT, CAN_RX	-	22	32	44

Name (Function after reset)	Type	I/O	Default multiplexing function	Additional function	QFN32	LQFP48	LQFP64
PA12	I/O	STD	USART1_RTS, TMR1_ETR, TMR4_CH4, EVENTOUT, CAN_TX	-	23	33	45
PA13 ⁽¹⁾ (SWDIO)	I/O	STD	SWDIO	-	24	34	46
PF6	I/O	STD	TMR1_CH4	-	-	35	47
PF7	I/O	STD	TMR2_CH2	-	-	36	48
PA14 ⁽¹⁾ (SWCLK)	I/O	STD	USART2_TX, SWCLK	-	25	37	49
PA15	I/O	STD	SPI1_NSS, USART2_RX, TMR2_CH1, EVENTOUT	-	26	38	50
PC10	I/O	STD	TMR1_CH1	-	-	-	51
PC11	I/O	STD	TMR1_CH2	-	-	-	52
PC12	I/O	STD	TMR1_CH3	-	-	-	53
PD2	I/O	STD	TMR1_CH4	-	-	-	54
PB3	I/O	STD	SPI1_SCK, EVENTOUT, TMR2_CH2	-	27	39	55
PB4	I/O	STD	SPI1_MISO, TMR3_CH1	-	28	40	56
PB5	I/O	STD	SPI1_MOSI, TMR3_CH2	-	29	41	57
PB6	I/O	STD	USART1_TX, TMR3_CH4	-	30	42	58
PB7	I/O	STD	USART1_RX, TMR3_CH3	-	31	43	59
PB11	I/O	STD	TMR2_CH4, EVENTOUT	-	-	44	60
PB8	I/O	STD	TMR4_CH3, CAN_RX	-	32	45	61
PB9	I/O	STD	TMR4_CH4, CAN_TX	-	-	46	62
VSS	P	-	VSS	VSS	0	47	63
LDO_CAP	P	-	LDO_CAP	LDO_CAP	-	48	64

Note:

- (1) After reset, these pins are configured for the SWDIO and SWCLK multiplexing functions, and the internal pull-up on the SWDIO pin and the internal pull-down on the SWCLK pin are activated.

3.3 GPIO Multiplexing Function Configuration

Table 4 GPIOA Multiplexing Function Configuration

Name	AF0	AF1	AF2	AF3	AF4	AF5	AF6
PA0	-	USART2_CTS	TMR2_CH1	-	CAN_RX	-	-
PA1	EVENTOUT	USART2_RTS	TMR2_CH2	-	CAN_TX	TMR4_CH2	-
PA2	TMR4_CH1	USART2_TX	TMR2_CH3	-	-	-	-
PA3	TMR4_CH2	USART2_RX	TMR2_CH4	-	-	-	-
PA4	SPI1_NSS	USART2_CK	-	TMR4_CH1	-	-	-
PA5	SPI1_SCK	-	TMR2_CH1	-	-	-	-
PA6	SPI1_MISO	TMR3_CH1	TMR1_BKIN	-	CAN_RX	TMR4_CH3	EVENTOUT
PA7	SPI1_MOSI	TMR3_CH2	TMR1_CH1N	-	CAN_TX	TMR4_CH4	EVENTOUT
PA8	MCO	USART1_CK	TMR1_CH1	EVENTOUT	-	-	-
PA9	TMR4_CH3	USART1_TX	TMR1_CH2	-	-	-	-
PA10	-	USART1_RX	TMR1_CH3	-	-	-	-
PA11	EVENTOUT	USART1_CTS	TMR1_CH4	-	CAN_RX	-	-
PA12	EVENTOUT	USART1_RTS	TMR1_ETR	TMR4_CH4	CAN_TX	-	-
PA13	SWDIO	-	-	-	-	-	-
PA14	SWCLK	USART2_TX	-	-	-	-	-
PA15	SPI1_NSS	USART2_RX	TMR2_CH1	EVENTOUT	-	-	-

Table 5 GPIOB Multiplexing Function Configuration

Name	AF0	AF1	AF2	AF3
PB0	USART1_TX	TMR3_CH3	TMR1_CH2N	-
PB1	USART1_RX	TMR3_CH4	TMR1_CH3N	-
PB2	-	-	TMR1_CH1N	-
PB3	SPI1_SCK	EVENTOUT	TMR2_CH2	-
PB4	SPI1_MISO	TMR3_CH1	-	-
PB5	SPI1_MOSI	TMR3_CH2	-	-
PB6	USART1_TX	-	TMR3_CH4	-
PB7	USART1_RX	-	TMR3_CH3	-
PB8	-	CAN_RX	TMR4_CH3	-
PB9	-	CAN_TX	TMR4_CH4	-
PB10	-	EVENTOUT	TMR2_CH3	-
PB11	EVENTOUT	-	TMR2_CH4	-
PB12	-	EVENTOUT	TMR1_BKIN	-
PB13	-	TMR2_CH4	TMR1_CH1N	-
PB14	-	TMR4_CH1	TMR1_CH2N	-
PB15	TMR2_CH3	TMR4_CH2	TMR1_CH3N	-

Table 6 GPIOC Multiplexing Function Configuration

Name	AF0	AF1	AF2	AF3
PC0	EVENTOUT	USART2_TX	-	-
PC1	EVENTOUT	USART2_RX	-	-
PC2	EVENTOUT	-	-	-
PC3	EVENTOUT	-	-	-
PC4	EVENTOUT	-	-	-
PC5	-	-	TMR1_CH4	-
PC6	TMR3_CH1	-	-	-
PC7	TMR3_CH2	-	-	-
PC8	TMR3_CH3	-	-	-
PC9	TMR3_CH4	-	-	-
PC10	-	-	TMR1_CH1	-
PC11	-	-	TMR1_CH2	-
PC12	-	-	TMR1_CH3	-
PC13	-	-	TMR1_CH1	-
PC14	-	-	TMR1_CH2	-
PC15	-	-	TMR1_CH3	-

Table 7 GPIOD & GPIOF Multiplexing Function Configuration

Name	AF0	AF1	AF2	AF3
PF0	-	-	-	-
PF1	-	-	-	-
PF4	EVENTOUT	-	-	-
PF5	EVENTOUT	-	-	-
PF6	TMR1_CH4	-	-	-
PF7	TMR2_CH2	-	-	-
PD2	-	-	TMR1_CH4	-

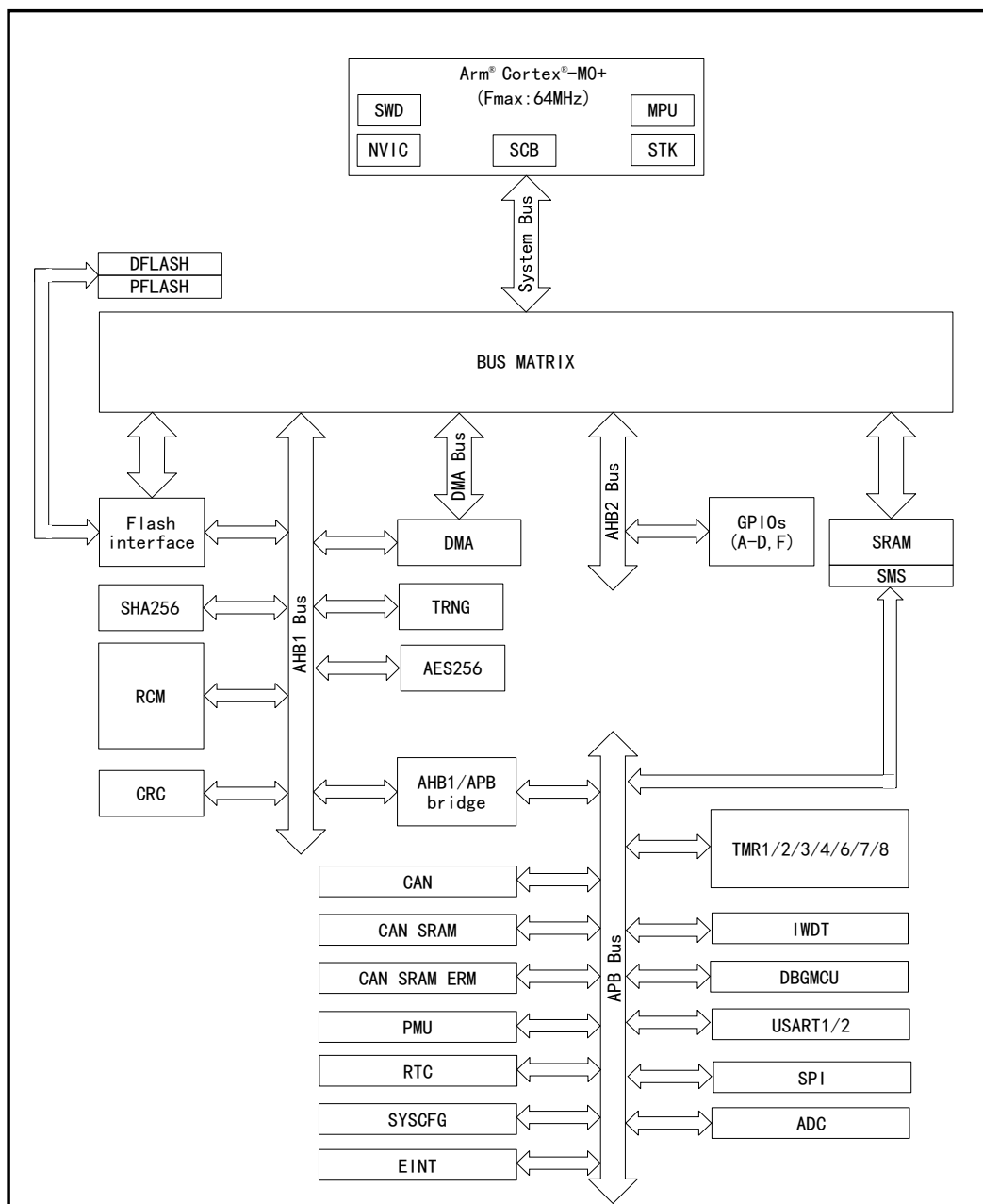
4 Functional Description

This chapter describes the system architecture, interrupts, on-chip memory, clock, power supply, and peripheral features of the G32A1085 A1065 A1045 family of products. For information about the Arm® Cortex® -M0+ core, refer to the *Arm® Cortex® -M0+ Technical Reference Manual*, which can be downloaded from Arm's website.

4.1 System architecture

4.1.1 System block diagram

Figure 4 G32A1085 A1065 A1045 System Block Diagram



4.1.2 Address mapping

Table 8 G32A1085 A1065 A1045 Address Mapping

Region	Start Address	Peripheral Name
Code	0x0000 0000	Code mapping area
Code	0x0004 0000	Reserved
Code	0x0800 0000	Main memory area
DFlash	0x0804 0000	Data storage area
Code	0x1FFF C800	Reserved
Code	0x1FFF F800	Option byte
Code	0x1FFF FC00	Reserved
SRAM	0x2000 0000	SRAM
APB bus	0x4000 0000	TMR2
APB bus	0x4000 0400	TMR3
APB bus	0x4000 0800	Reserved
APB bus	0x4000 0C00	Reserved
APB bus	0x4000 1000	TMR6
APB bus	0x4000 1400	Reserved
APB bus	0x4000 1800	Reserved
APB bus	0x4000 2000	TMR4
APB bus	0x4000 2400	Reserved
APB bus	0x4000 2800	RTC
APB bus	0x4000 2C00	Reserved
APB bus	0x4000 3000	IWDT
APB bus	0x4000 3400	Reserved
APB bus	0x4000 3800	Reserved
APB bus	0x4000 3C00	Reserved
APB bus	0x4000 4400	USART2
APB bus	0x4000 4800	Reserved
APB bus	0x4000 4C00	Reserved
APB bus	0x4000 5000	Reserved
APB bus	0x4000 5400	SRAM ERM
APB bus	0x4000 5800	CAN SRAM ERM(ERP)
APB bus	0x4000 5C00	CAN SRAM (0x4000 5C00-0x4000 63FF)
APB bus	0x4000 6400	CAN
APB bus	0x4000 6C00	Reserved
APB bus	0x4000 7000	PMU
APB bus	0x4000 7400	Reserved
APB bus	0x4000 7800	Reserved

Region	Start Address	Peripheral Name
APB bus	0x4000 7C00	Reserved
—	0x4000 8000	Reserved
APB bus	0x4001 0000	SYSCFG
APB bus	0x4001 0400	EINT
APB bus	0x4001 0800	Reserved
APB bus	0x4001 2400	ADC
APB bus	0x4001 2800	Reserved
APB bus	0x4001 2C00	TMR1
APB bus	0x4001 3000	SPI
APB bus	0x4001 3400	Reserved
APB bus	0x4001 3800	USART1
APB bus	0x4001 3C00	Reserved
APB bus	0x4001 4000	TMR7
APB bus	0x4001 4400	TMR8
APB bus	0x4001 4800	Reserved
APB bus	0x4001 4C00	Reserved
APB bus	0x4001 5800	DBGMCU
APB bus	0x4001 5C00	Reserved
—	0x4001 8000	Reserved
AHB1 bus	0x4002 0000	DMA
AHB1 bus	0x4002 0400	Reserved
AHB1 bus	0x4002 1000	RCM
AHB1 bus	0x4002 1400	Reserved
AHB1 bus	0x4002 2000	Flash interface
AHB1 bus	0x4002 2400	Reserved
AHB1 bus	0x4002 3000	CRC
AHB1 bus	0x4002 3400	Reserved
AHB1 bus	0x4002 4000	Reserved
AHB1 bus	0x4002 4400	Reserved
AHB1 bus	0x4002 6000	AES256
AHB1 bus	0x4002 6400	SHA256
AHB1 bus	0x4002 6800	TRNG
AHB2 bus	0x4800 0000	GPIOA
AHB2 bus	0x4800 0400	GPIOB
AHB2 bus	0x4800 0800	GPIOC
AHB2 bus	0x4800 0C00	GPIOD
AHB2 bus	0x4800 1000	Reserved
AHB2 bus	0x4800 1400	GPIOF

Region	Start Address	Peripheral Name
—	0x4800 1800	Reserved
Core	0xE000 E010	STK
Core	0xE000 E100	NVIC
Core	0xE000 ED00	SCB
—	0xE010 0000	Reserved

4.2 Core

The core of G32A1085 A1065 A1045 is an Arm® Cortex® -M0+, the latest generation of embedded Arm cores, based on a low-cost, low-power development platform that delivers excellent computational performance and advanced system interrupt response, compatible with all Arm tools and software.

4.3 Interrupt controller

4.3.1 Nested Vector Interrupt Controller (NVIC)

G32A1085 A1065 A1045 has a built-in Nested Vector Interrupt Controller (NVIC), which is capable of handling up to 32 maskable interrupt channels (excluding 16 Arm® Cortex® -M0+ interrupt lines) and 4 priority levels. The interrupt vector entry address can be passed directly to the core to achieve a low-latency interrupt response that can prioritize late arriving higher priority interrupts.

4.3.2 External Interrupt/Event Controller (EINT)

External interrupt/event controller has 32 edge detectors. Each detector contains edge detection circuitry, interrupt/event request generation circuitry. Each detector can be configured as a rising-edge triggered, falling-edge triggered or double-edge triggered, but also able to be individually masked. Up to 55 GPIOs can be connected to 16 external interrupt lines.

4.4 On-chip memory

User-modifiable memory includes main memory, data storage area, SRAM, and option bytes. System memory stores 96-bit unique device ID, main memory capacity information, and data memory capacity information.

The PFlash, DFlash and SRAM storage areas all have ECC, which can correct single-bit errors and detect double-bit errors.

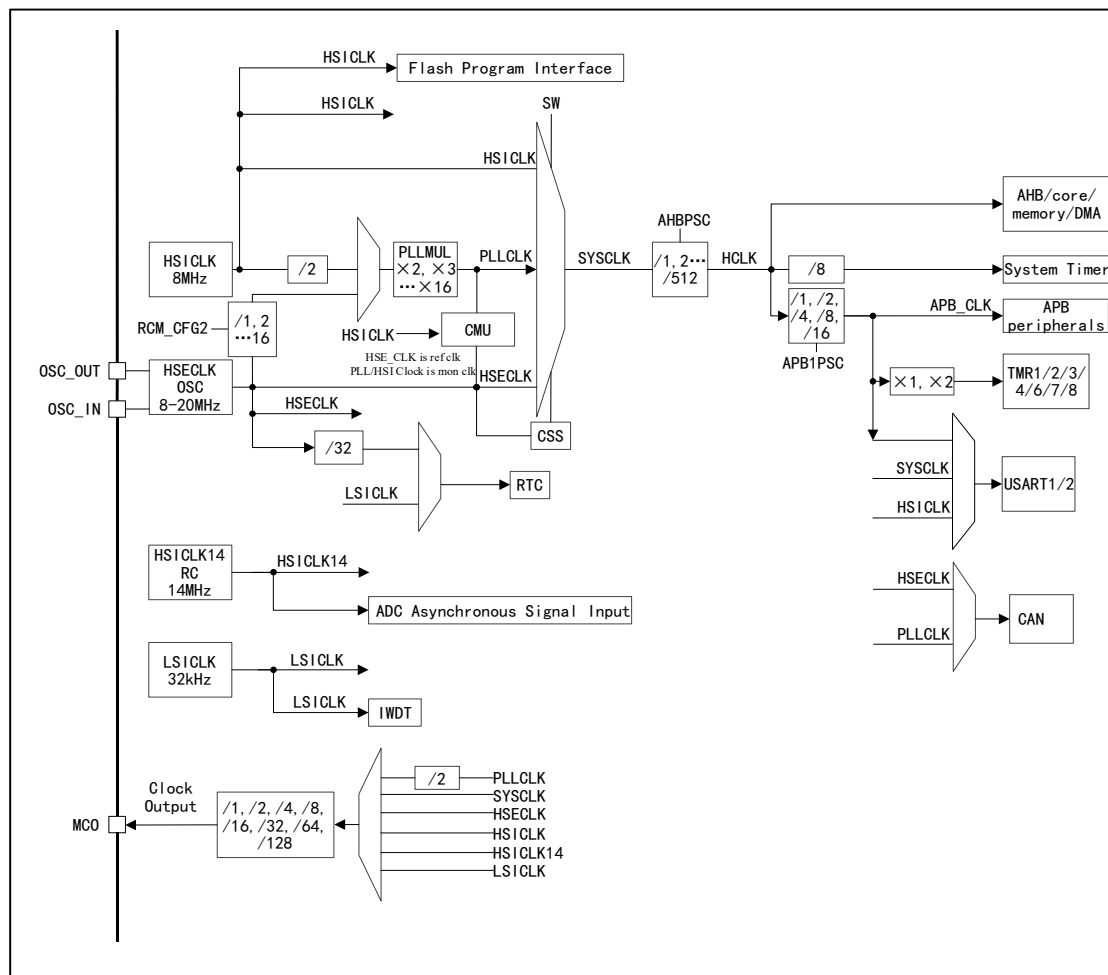
Table 9 Memory Description

Memory	G32A1085 Maximum bytes	G32A1065 Maximum bytes	G32A1045 Maximum bytes	Description
PFlash	256KB	128KB	64KB	Store user code and constant data
DFlash	32KB	32KB	16KB	Store data
SRAM	32KB	16KB	8KB	—
Option bytes	24Bytes	24Bytes	24Bytes	Configure main memory read/write protection, MCU operating mode

4.5 Clock

The clock tree of G32A1085 A1065 A1045 is shown in the figure below:

Figure 5 G32A1085 A1065 A1045 Clock Tree



4.5.1 Clock sources

The clock source of G32A1085 A1065 A1045 is divided into high-speed clock and low-speed clock. High-speed clock has HSI14, HSI14, HSECLK, and

low-speed clock has LSICLK.

By on-chip/off-chip, the clock is divided into internal clock and external clock. Internal clock has HSICLK14, HSICLK, LSICLK, and external clock has HSECLK. For HSICLK14 and HSICLK, they will be calibrated at the factory.

4.5.2 System clock

G32A1085 A1065 A1045 can select HSICLK, PLLCLK, HSECLK as the system clock; the clock source of HSICLK is HSICLK; the clock source of PLLCLK can be selected from one of HSICLK and HSECLK, and configure the PLL's multiplying factor and dividing factor to obtain the desired system clock; the clock source of HSECLK is HSECLK. When the product is reset and started, HSICLK is selected as the system clock by default. Afterwards, users can choose one of the above three clock sources as the system clock.

4.5.3 Bus clock

Built-in AHB and APB buses. The clock source of AHB is the result of SYSCLK frequency division. The clock source of APB is the result of HCLK frequency division. The maximum frequency of AHB and APB is 64MHz.

4.6 Power management

4.6.1 Power supply scheme

Table 10 Power supply scheme

Name	Voltage range	Description
V _{DD}	2.75~5.5V	Power supply to I/O, internal regulator through VDD pin. RC oscillator and PLL are powered by internal 3.3V regulator.
V _{DDA}	V _{DD} ~5.5V	V _{DDA} powers the ADC and reset modules, and the V _{DDA} voltage level must always be greater than or equal to the V _{DD} voltage.

Note: For more detailed information on how to connect the power supply pins, see the figure "Power Supply Scheme".

4.6.2 Voltage regulators

Table 11 Regulator Operating Modes

Name	Description
Master Mode (MR)	Used in run mode
Low-power mode (LPR)	Used in stop mode
Power-down mode	Used in standby mode. The voltage regulator provides high-impedance output and the core circuit is powered down. The power consumption of the voltage regulator is zero, and all data of registers and SRAM will be lost.

4.6.3 Power supply monitor

Power-on reset (POR) and power-down reset (PDR) circuits are integrated inside the product. Both circuits are always in the working status. When the power-down reset circuit monitors that the power supply voltage is below a specified threshold ($V_{POR/PDR}$), the system maintains the reset state even if an external reset circuit is used.

The product has a built-in programmable voltage regulator (PVD) that monitors V_{DD} and compares it to the V_{PVD} threshold. An interrupt is generated when V_{DD} is outside the V_{PVD} threshold range and an interrupt is enabled, allowing the MCU to be set to a safe state through the interrupt service program.

4.7 Low-power mode

G32A1085 A1065 A1045 supports sleep, stop and standby mode.

Table 12 Low-power Modes

Mode	Description
Sleep mode	The core stops working. All peripherals are working. Can be woken up through interrupts/events.
Stop mode	The stop mode achieves the lower power consumption without loss of SRAM and register data. The clocks of the internal 1.2V powered modules are all stopped. The HSECLK crystal oscillator, HSICLK, and PLL are disabled, and the regulator can be configured for either normal mode or low-power mode. For the lowest power consumption, the 1.2V and 3.3V regulators need to be put into LP mode (LPDSCFG set to 1). Any external interrupt line can wake up the MCU. External interrupt lines include one of the 16 EINT signal lines, USART1, USART2, CAN, RTC.
Standby mode	This mode achieves the lowest power consumption. The internal voltage regulator is disabled, and all 1.2V power modules are powered down. The HSECLK crystal oscillator, HSICLK, and PLL clocks are shut down. SRAM and register contents are lost, while the standby circuitry remains active. The MCU exits the standby mode through an external reset on the NRST pin, an IWDG reset, or an RTC alarm event.

Note: The IWDG and the corresponding clock still work normally in sleep, stop or standby mode.

4.8 GPIO

The GPIOs can be configured as general-purpose inputs, general-purpose outputs, multiplexed functions, and analog modes. General-purpose inputs can be configured as float, pull-up, and pull-down. General-purpose outputs can be configured as push-pull and open-drain outputs. Multiplexing function can be used for digital peripherals. Analog mode can be used for analog peripherals.

Enabling/disabling pull-up/pull-down resistors can be configured. The speed can be configured to be low 2 MHz, medium 10 MHz, and high 20 MHz. The higher the speed, the higher the power consumption and the noise will be.

4.9 Communication interface

4.9.1 USART

The chip built-in up to 2 universal synchronous / asynchronous transceiver, communication rate up to support 8Mbit/s. All USART can be configured baud rate, parity bit, stop bit, and data bit length. The DMA controller can be used. Support for single-wire half-duplex mode. The differences of each USART function are shown in the table below:

Table 13 G32A1085 A1065 A1045 USART Function Differences

USART mode/function	USART1	USART2
Hardware flow control of modem	√	√
Synchronous mode	√	√
Multi-processing communication	√	√
LIN mode	√	√
Dual clock domains and wake-up from stop mode	√	√
Receiver timeout interrupt	√	√
Automatic baud rate detection	√	√

Note: √ means supported.

4.9.2 SPI

Built-in 1 SPI, supports full-duplex and half-duplex communication in both master and slave modes. DMA controller can be used. 4~16 bits per frame can be configured, and the communication rate is up to 16Mbit/s.

4.9.3 CAN

- ISO 11898-1:2015 compliant, supports CAN2.0A/B and CAN FD protocols
- Support CAN FD protocol with up to 64 bytes of data
- Equipped with CAN error logging function
- Support AUTOSAR (Automotive Open Systems Architecture)
- Support SAE J1939 protocol (communication protocol for commercial vehicles)
- Improved acceptance filtering
- Two configurable receive first-in-first-out (FIFO) buffers
- Independent signalling for high priority message reception
- Up to 64 dedicated receive buffers
- Up to 32 dedicated transmit buffers
- Configurable transmit FIFO buffers
- Configurable send queue

- Configurable send event FIFO buffer
- Direct CPU access to Message Random Access Memory (Message RAM)
- Programmable loopback test mode
- Maskable module interrupts
- Dual clock domain (CAN communication clock and CAN peripheral clock)
- Power-down mode and wake-up support
- SRAM ECC checksum support, checksum errors can trigger interrupts and support query error address
- Supports the maximum data bit rate of 8 Mbit/s

4.10 Analog peripherals

4.10.1 ADC

1 built-in 12-bit ADC, up to 16 external channels, 3 internal channels. The internal channels are used for temperature sensor, reference voltage, and internal power supply detection. ADC each channel A/D conversion mode supports single, continuous, scanning or intermittent.

4.10.2 Temperature sensor

1 built-in temperature sensor (TSensor), internally connected to the ADC_IN16 channel. The voltage generated by the sensor varies linearly with the temperature, and can be converted to temperature by acquiring the converted voltage value through the ADC.

Table 14 Temperature Sensor Calibration Values

Calibration name	Description	Memory address
T _{sensor_CAL1}	Raw data collected at temperature 25°C (±5°C) and V _{DDA} =5V(±10mV)	0x1FFF F454-0x1FFF F455
T _{sensor_CAL2}	Raw data collected at temperature -40°C (±5°C) and V _{DDA} =5V(±10mV)	0x1FFF F458-0x1FFF F459
T _{sensor_CAL3}	Raw data collected at temperature 125°C (±5°C) and V _{DDA} =5V(±10mV)	0x1FFF F45A-0x1FFF F45B

4.10.3 Internal reference voltage calibration

The internal reference voltage V_{REFINT}, is internally connected to the ADC_IN17 channel and can be obtained from the ADC. V_{REFINT} provides a stable voltage output for the ADC.

Table 15 Internal Reference Voltage Calibration Values

Calibration name	Description	Memory address
V _{REFINT_CAL}	Raw data collected at temperature 25°C (±5°C) and V _{DDA} =5V(±10mV)	0x1FFF F456-0x1FFF F457

4.10.4 Internal Power Monitoring

Internally connected to ADC_IN18 channel, voltage status can be read by register configuration, contains VDD_FLASH_1.7_32K, VDD_FLASH_1.7_256K, and VDD_CORE_1.2.

4.11 Timers

1 built-in 16-bit advanced timer TMR1, 3 16-bit general-purpose timers TMR2/3/4, 2 basic timers TMR6/7, 1 CAN timestamp timer TMR8, 1 independent watchdog timer (supporting window mode), and 1 system tick timer.

The watchdog timer can be used to check if the programme is running properly.

The system tick timer is a peripheral of the core with an auto-reload function that can generate a maskable system interrupt when the counter is 0. It can be used for both real-time operating systems and normal delays.

A comparison of their characteristics is shown below:

Table 16 Comparison of Advanced/General/Basic and System Tick Timer Functions

Timer Type	System Tick Timer	Basic Timer	General Timer	Advanced Timer
Timer name	SysTick Timer	TMR6/7/8	TMR2/3/4	TMR1
Counter resolution	24 bits	16 bits	16 bits	16 bits
Counter type	Down	Up	Up, Down, Up/Down	Up, Down, Up/Down
Prescaler factor	-	Any integer between 1 and 65536	Any integer between 1 and 65536	Any integer between 1 and 65536
Generate DMA request	-	TMR6/7 Yes TMR8 No	Yes	Yes
Capture/Compare channel	-	-	4	4
Complementary output	-	No	No	Yes
Pin characteristics	-	-	4 non-complementary channel pins	Total 9 pins: 1 external trigger signal input, 1 brake input signal, 3 pairs of complementary channels, 1 non-complementary channel
Function description	Dedicated to real-time operating systems. With automatic reload function.	Can be used as a 16-bit general-purpose time base counter.	Has 4 independent channels, each for input capture/compare, PWM or mono-pulse mode outputs. Each timer channel has an independent DMA request mechanism.	Has complementary PWM outputs with deadband insertion. Configured as a 16-bit standard timer, it has the same functionality as the TMRx timer. When configured as a 16-bit PWM generator, it has full modulation capability (0 to 100%). In debug mode, the counter can be frozen while the

Timer Type	System Tick Timer	Basic Timer	General Timer	Advanced Timer
	<p>Can generate a maskable system interrupt when the counter is 0.</p> <p>Programmable clock source.</p>			PWM output is disabled. Synchronization or event linking functions are provided.

Table 17 Independent Watchdog Timer

Name	Counter Resolution	Counter Type	Prescaler Factor	Function Description
Independent Watchdog	12 bits	Down	4, 8, 16, 32, 64, 128, 256	<p>Clocked by LSI. Can run in stop mode.</p> <p>Can reset the entire system in the event of a problem.</p> <p>Can be used as a free timer to provide timeout management for applications.</p> <p>Can be configured to be a software-initiated or hardware-initiated watchdog via option bytes.</p> <p>The counter can be frozen in debug mode.</p>

4.12 CRC computing unit

1 built-in CRC (Cyclic Redundancy Check) computing unit, which generates CRC codes and can operate on 8-bit, 16-bit, and 32-bit data.

4.13 DMA

1 built-in DMA, supporting 5 DMA channels. Each channel supports multiple DMA requests, but only 1 DMA request is allowed to enter the DMA channel at the same time. Peripherals that support DMA requests are: ADC, SPI, USART1/2, TMR1, TMR2, TMR3, TMR4, TMR6, TMR7. Support "Memory → Memory, Memory → Peripheral, Peripheral → Memory" data transfer (Memory including Flash and SRAM).

4.14 SMS

SMS provides ECC checks for SRAM, including error detection, single-bit error correction, and double-bit error detection. An additional parity bit is appended to each address. When ECC is enabled, SMS internally computes the parity bits on every write operation.

For every read operation, including RMW reads, any ECC error is reported and logged. Reported ECC errors can generate a masked system interrupt.

SMS can insert error bits during SRAM accesses for diagnostic purposes. It can be configured to inject single-bit errors, double-bit errors, and triple-bit errors.

4.15 TRNG

The TRNG is a true random number generator, based on continuous analog noise, for which a 32-bit random number is provided at the host readout. The interval between two successive random numbers is 40 clock signal cycles. Monitoring TRNG entropy to flag anomalous behaviour.

4.16 SHA256

SHA-256 (Secure Hash Algorithm 256-bit) is a cryptographic Hash function that is part of the SHA-2 family. Integrating the SHA256 module in the MCU can provide the system with efficient and secure Hash computation capability, which can be applied in security-related application scenarios such as data integrity verification, digital signature, and password storage.

- Support little-endian mode (0x64636261)
- Support SHA256 algorithm
- Support segmented computing

- Support single-block computation only. When performing a multi-block calculation, the result of the previous calculation must be entered into the DIGEST register of the current Hash calculation.

4.17 **AES256**

The encryption processor uses the AES algorithm to encrypt and decrypt data to be transmitted.

- Support ECB, CBC and CTR link algorithms
- Support encryption, decryption, and key expansion
- Support 128-bit, 192-bit, and 256-bit keys
- Support CMAC algorithms, including subkey generation and MAC generation

5 Electrical Characteristics

5.1 Test conditions of electrical characteristics

All voltage parameters (unless otherwise stated) are referenced to V_{SS} .

5.1.1 Maximum and minimum values

Unless otherwise specified, all products are tested on the production line at $T_A=25^\circ\text{C}$. Its maximum and minimum values can support the worst environmental temperature, power supply voltage and clock frequency.

5.1.2 Typical value

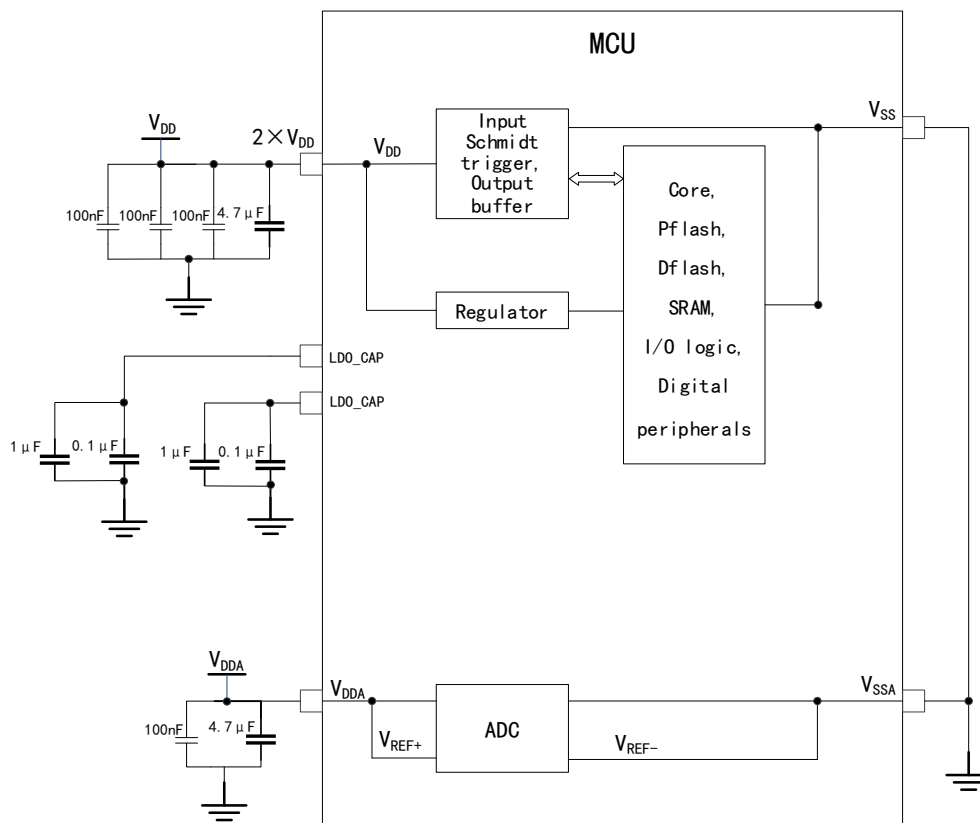
Unless otherwise specified, typical data are measured based on $T_A=25^\circ\text{C}$, $V_{DD}=V_{DDA}=5\text{V}$. These data are only used for design guidance.

5.1.3 Typical curve

Unless otherwise specified, typical curves are only used for design guidance and are not tested.

5.1.4 Power supply scheme

Figure 6 Power Supply Scheme



5.1.5 Load capacitance

Figure 7 Load conditions when measuring pin parameters

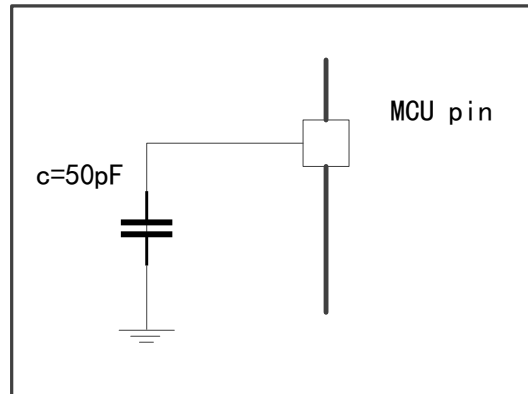


Figure 8 Pin Input Voltage Measurement Scheme

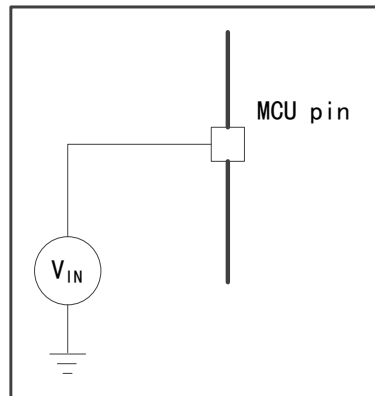
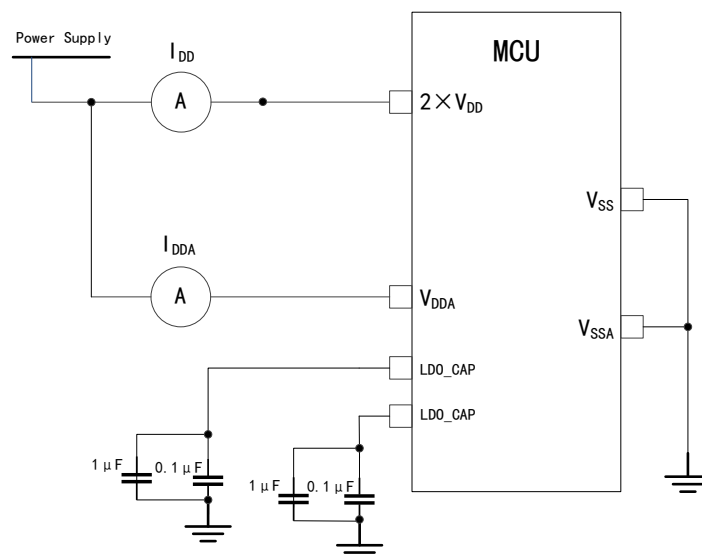


Figure 9 Power Consumption Measurement Scheme



5.2 Test under general operating conditions

Table 18 General Operating Conditions

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
f_{HCLK}	Internal AHB clock frequency	-	-	-	64	MHz
f_{PCLK}	Internal APB clock frequency	-	-	-	64	
V_{DD}	Standard Operating Voltage	-	2.75	-	5.5	V
V_{DDA}	Analog operating voltage	V_{DDA} must not be less than V_{DD}	2.75	-	5.5	
V_{IN}	I/O input voltage	STD and RST I/O	-0.3	-	$V_{DD}+0.3$	
		STDA I/O	-0.3	-	$V_{DDA}+0.3$	

5.3 Absolute maximum ratings

Loads on the device that exceed the absolute maximum ratings may cause permanent damage to the device. The maximum loads that can be applied are provided here and do not guarantee that the device will function properly under these conditions.

5.3.1 Maximum temperature characteristics

Table 19 Temperature Characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-65~+150	°C
T_A	Ambient temperature	-40~+125	

5.3.2 Maximum rated voltage characteristics

All power supply (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the power supply within the external limited range.

Table 20 Maximum Rated Voltage Characteristics

Symbol	Description	Minimum value	Maximum value	Unit
$V_{DD}-V_{SS}$	External main supply voltage (V_{DD})	-0.3	5.8	V
$V_{DDA}-V_{SSA}$	External analog supply voltage (V_{DDA})	-0.3	5.8	
$V_{DD}-V_{DDA}$	$V_{DD}>V_{DDA}$ allowable voltage difference	-	0.4	
V_{IN}	Input voltage on pins	$V_{SS}-0.3$	5.8	
$ \Delta V_{DDx} $	Voltage difference between supply pins	-	50	mV

Symbol	Description	Minimum value	Maximum value	Unit
$ V_{SSx}-V_{SS} $	Voltage difference between ground pins	-	50	

5.3.3 Maximum rated current characteristics

Table 21 Maximum Rated Current Characteristics

Symbol	Description	Maximum value	Unit
ΣI_{VDD}	Total current through V_{DD}/V_{DDA} power lines ⁽¹⁾	120	mA
ΣI_{VSS}	Total current through V_{SS} ground lines ⁽¹⁾	-120	
$I_{VDD (PIN)}$	Maximum current into each V_{DD}/V_{DDA} supply pin ⁽¹⁾	100	
$I_{VSS (PIN)}$	Maximum current into each V_{SS} ground pin ⁽¹⁾	-100	
$I_{INJ(PIN)}^{(3)}$	Current injection on STD pin and RST pin	-5/+0 ⁽⁴⁾	
	Current injection at STDA pin ⁽⁴⁾	± 5	
$\Sigma I_{INJ(PIN)}^{(2)}$	Total injected current on all I/O and control pins ⁽⁵⁾	± 25	

Note:

- (1) All power supply (V_{DD}, V_{DDA}) and ground (V_{SS}, V_{SSA}) must always be within the allowed range.
- (2) If V_{IN} exceeds the maximum value, $I_{INJ(PIN)}$ must be externally limited to not exceed its maximum value. When $V_{IN} > V_{DD}$, current flows into the pin; when $V_{IN} < V_{SS}$, current flows out of the pin.
- (3) Positive injection is not possible on these I/Os and does not occur when the input voltage is below the specified maximum.
- (4) On these I/Os, $V_{IN} > V_{DDA}$ induces positive injection. Negative injection interferes with the analog performance of the device.
- (5) When multiple inputs are submitted to a single current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute (instantaneous) value of the injected positive and negative currents.

5.3.4 ESD characteristics

Table 22 ESD Characteristics ⁽¹⁾

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (Human body model) $V_{DD}, V_{DDA},$ LDO_CAP pins	$T_A = +25^\circ C$, conforming to ANSI/ESDA/JEDEC JS- 001-2017	-4000	4000	V
	Electrostatic discharge voltage (Human body model) Other pins		-6000	6000	

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
V _{ESD(CDM)}	Electrostatic discharge voltage (Charged device model)	T _A =+25°C, conforming to ANSI/ESDA/JEDEC JS-002-2018	-1000	1000	

Note: (1) The samples are measured by a third-party testing organization and are not tested in production. Ensure the power is completely turned off before handling the chip. Do not handle under power to prevent hardware damage.

5.3.5 Static latch-up (LU)

Table 23 Static Latch-up⁽¹⁾

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
LU	Class of static latch-up	T _A =+125°C	-200	200	mA
		T _A =+25°C	-200	200	

Note: (1) The samples are measured by a third-party testing organization and are not tested in production.

5.4 On-chip memory

5.4.1 Flash characteristics

Table 24 Flash Characteristics⁽¹⁾

Symbol	Parameter	Conditions	Minimum value	Typical value	Maximum value	Unit
t _{prog}	64-bit programming time	T _A =-40~125°C, V _{DD} =2.75~5.5V	-	215	-	μs
t _{ERASE}	Page (512B) erase time	T _A =-40~125°C, V _{DD} =2.75~5.5V	-	4	-	ms
t _{ME}	Mass erase time	T _A =25°C, V _{DD} =2.75~5.5V	-	10	-	ms
V _{prog}	Programming voltage	T _A =-40~125°C	2.75	-	5.5	V
t _{RET}	Data retention time	T _A =25°C	-	20	-	years
N _{RW}	Erase write cycle	T _A =25°C	-	100K	-	cycles
-	Fastest execution time for zero-wait-cycle Flash	T _A =-40~125°C, V _{DD} =2.75~5.5V	-	-	24	MHz

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.5 Clock

5.5.1 External clock source characteristics

High-speed external clock generated by crystal oscillator

For detailed parameters (frequency, package, precision, and so on) of crystal oscillator, consult the corresponding manufacturers.

Table 25 HSECLK 8~20MHz Oscillator Characteristics⁽¹⁾

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
f _{OSC_IN}	Oscillator frequency	-	8	16	20	MHz
R _F	Feedback resistance	-	-	500	-	kΩ
I _{start}	Start-up drive current	-	1.12	1.47	2.02	mA
I _{DD}	HSECLK current consumption	C _L =8pF@8MHz	-	0.54	-	
I _{DD}	HSECLK current consumption	C _L =6pF@16MHz	-	0.55	-	
I _{DD}	HSECLK current consumption	C _L =10pF@20MHz	-	0.85	-	
g _m	Oscillator transconductance 8-20M	Startup	6.6	10	13.3	mA/V
t _{SU} (HSECLK)	Start-up time	Stable V _{DD}	-	2	-	ms

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

Recommended oscillator crystal configuration

Static capacitance C₀≤3pF, load capacitance C_L≤12pF, 8M crystal oscillator resistor R_r≤300Ω, 16M crystal oscillator resistor R_r≤80Ω, 20M crystal oscillator resistor R_r≤80Ω, excitation power D_L≤100μW.

5.5.2 Internal clock source characteristics

High-speed internal (HSICLK) RC oscillator

Table 26 HSICLK Oscillator Characteristics

Symbol	Parameter	Condition		Min value	Typ value	Max value	Unit
f _{HSICLK}	Frequency	-		-	8	-	MHz
ACCHSICLK	HSICLK oscillator accuracy	Factory calibrated	V _{DD} =3.3V/5V, T _A =25°C ⁽¹⁾	-1	-	1	%
			V _{DD} =2.75-5.5V,	-2.5	-	2.5	%

Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
		$T_A = -40 \sim 125^\circ\text{C}$				
$t_{\text{SU}}(\text{HSICLK})$	HSICLK oscillator start-up time	$V_{\text{DD}} = 3.3\text{V}/5\text{V}$ $T_A = -40 \sim 125^\circ\text{C}$	1	-	2	μs
$I_{\text{DDA}}(\text{HSICLK})$	HSICLK oscillator power consumption	-	-	100	150	μA

Note: With the exception of (1) which is calibrated in production, the other data is derived from a comprehensive evaluation and is not tested in production.

Table 27 HSICLK14 Oscillator Characteristics

Symbol	Parameter	Condition	Min value	Typ value	Max value	Unit
f_{HSICLK14}	Frequency	-	-	14	-	MHz
$ACCHSICLK14$	HSICLK14 oscillator accuracy	Factory calibrated $V_{\text{DD}} = 3.3\text{V}/5\text{V}$, $T_A = 25^\circ\text{C}^{(1)}$	-1	-	1	%
		$V_{\text{DD}} = 2.75\text{-}5.5\text{V}$, $T_A = -40 \sim 125^\circ\text{C}$	-4.2	-	5.1	%
$t_{\text{SU}}(\text{HSICLK14})$	HSICLK14 oscillator start-up time	$V_{\text{DD}} = 3.3\text{V}/5\text{V}$ $T_A = -40 \sim 125^\circ\text{C}$	1	-	2	μs
$I_{\text{DDA}}(\text{HSICLK14})$	HSICLK14 oscillator power consumption	-	-	100	150	μA

Note: With the exception of (1) which is calibrated in production, the other data is derived from a comprehensive evaluation and is not tested in production.

Low-speed internal (LSICLK) RC oscillator

Table 28 LSICLK Oscillator Characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit	
f_{LSICLK}	Frequency ($V_{\text{DD}} = 2.75\text{-}5.5\text{V}$, $T_A = -40 \sim 125^\circ\text{C}$)	30.4	32	33.6	kHz	
$ACCLSICLK$	LSICLK oscillator accuracy ⁽¹⁾	$T_A = -40 \sim 125^\circ\text{C}$	-5	-	5	%
		$T_A = 25^\circ\text{C}$	-3	-	3	

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
$t_{SU(LSICLK)}$	LSICLK oscillator start-up time ($V_{DD}=3.3V/5V$, $T_A=-40\sim 125^{\circ}C$)	-	-	128	μs
$I_{DD(LSICLK)}$	LSICLK oscillator power consumption	-	0.4	1.2	μA

Note: With the exception of (1) which is calibrated in production, the other data is derived from a comprehensive evaluation and is not tested in production.

5.5.3 PLL characteristics

Table 29 PLL Characteristics ⁽¹⁾

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
f_{PLL_IN}	PLL input clock	1	8.0	24	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock ($V_{DD}=3.3V/5V$, $T_A=-40\sim 125^{\circ}C$)	-	64	-	MHz
t_{LOCK}	PLL phase lock time	-	-	200	μs

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.6 Power management

5.6.1 Embedded Reset and Power Control Module Characteristics Test

Table 30 Embedded Reset and Power Control Module Characteristics ⁽¹⁾

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{POR}	Power-on reset threshold	Falling edge	1.65	1.7	1.9	V
		Rising edge	1.85	1.9	2.0	
V_{PDR}	Power-down reset threshold	Falling edge	2.4	2.48	2.65	
		Rising edge	2.52	2.6	2.74	
$V_{PORhyst}$	POR hysteresis	-	-	200	-	mV
$V_{PDRhyst}$	PDR hysteresis	-	-	120	-	
$T_{RSTTEMPO}$	POR hysteresis time	-	0.67	2	5	ms
T_{PDR}	PDR filter delay	-	10	20	44	μs
V_{LDO_CAP}	LDO_CAP output voltage	Running mode	3.1	3.3	3.5	V
		Low power consumption mode	2.48	2.6	2.85	
$LDO_CAP^{(2)}$	LDO filter capacitor	-	1	2.2	10	μF
Tramp_MCU	MCU power-up slope	-	0.5V/min	-	100V/ms	-
Tramp_ECU	ECU power-up slope	-	0.5V/min	-	500V/ms	-

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V _{REFINT}	Built-in reference voltage	-40°C < T _A < +125°C	-	1.23 ⁽³⁾	-	V

Note:

- (1) The data are obtained from a comprehensive evaluation and are not tested in production.
- (2) Connect a filter capacitor to each LDO_CAP pin, as close as possible to the chip pins. Recommended capacitance: For LQFP64 and LQFP48 packages, each of the two LDO_CAP pins should be connected to a 1μF capacitor. For the QFN32 package, the single LDO_CAP pin should be connected to a 2.2μF capacitor.
- (3) Due to internal circuit coupling, the V_{REFINT} value obtained via ADC sampling may deviate from the actual value (whereas the directly measured value at the pin is within the specified range). It is recommended to use multiple-sample averaging in applications to improve measurement accuracy.

Table 31 Programmable Voltage Detector Characteristics⁽¹⁾

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V _{PVD}	Programmable voltage detector level selection	PLS[2:0]=000 (Falling edge)	2.50	2.73	2.85	V
		PLS[2:0]=000 (Rising edge)	2.70	2.87	2.98	V
		PLS[2:0]=001 (Falling edge)	2.50	2.73	2.85	V
		PLS[2:0]=001 (Rising edge)	2.70	2.87	2.98	V
		PLS[2:0]=010 (Falling edge)	2.80	3.05	3.15	V
		PLS[2:0]=010 (Rising edge)	3.04	3.20	3.34	V
		PLS[2:0]=011 (Falling edge)	3.10	3.37	3.45	V
		PLS[2:0]=011 (Rising edge)	3.34	3.50	3.68	V
		PLS[2:0]=100 (Falling edge)	3.40	3.66	3.75	V
		PLS[2:0]=100 (Rising edge)	3.62	3.79	3.92	V
		PLS[2:0]=101 (Falling edge)	3.70	3.95	4.08	V
		PLS[2:0]=101 (Rising edge)	3.92	4.08	4.28	V
		PLS[2:0]=110 (Falling edge)	4.10	4.26	4.40	V
		PLS[2:0]=110 (Rising edge)	4.21	4.37	4.50	V
PLS[2:0]=111 (Falling edge)	4.30	4.52	4.65	V		
PLS[2:0]=111 (Rising edge)	4.46	4.64	4.78	V		
V _{PVDhyst}	PVD hysteresis	-	-	120	-	mV

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.7 Power consumption

5.7.1 Power consumption test

- (1) Execute with Coremark, compiled with Keil V5 and compiled with the highest optimization level of L0.
- (2) All I/O pins configured as analog inputs are connected to a static level on V_{DD} or V_{SS} (no load).
- (3) Unless otherwise noted, all peripherals are turned off.
- (4) The relationship between Flash wait cycle setting and f_{HCLK} :
 - 0~24MHz: 0 wait cycle
 - 24~48MHz: 1 wait cycle
 - 48~64MHz: 2 wait cycles
- (5) When peripherals are enabled: $f_{PCLK}=f_{HCLK}$

Table 32 Power Consumption in Standby and Stop modes⁽¹⁾

Working mode	Condition	-40°C		25°C		105°C		125°C		Unit
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	
STANDBY1	LSI and IWDWT ON	9.91	14	10.46	14	14.42	28	20.17	30	μA
STANDBY2	LSI and IWDWT OFF	9.37	14	9.91	14	13.91	28	19.65	30	
STOP1	Peripherals OFF, Regulator ON	253.08	290	262.00	290	349.23	400	441.74	500	
STOP2	Peripherals OFF, Regulator OFF	25.97	50	31.17	50	112.83	200	207.05	280	

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

Table 33 Power Consumption in Sleep Mode⁽¹⁾

Working mode	Condition	-40°C		25°C		105°C		125°C		Unit
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	
HSECLK16, enabling all peripherals ⁽²⁾	f _{HCLK} =64MHz	5.65	8	5.70	8	5.75	8	5.88	8	mA
HSECLK16, disabling all peripherals	f _{HCLK} =64MHz	2.51	5	2.55	5	2.60	5	2.71	5	
HSICLK, enabling all peripherals ⁽²⁾	f _{HCLK} =64MHz	4.95	8	5.10	8	5.22	8	5.34	8	
HSICLK, disabling all peripherals	f _{HCLK} =64MHz	1.86	5	1.91	5	2.09	5	2.20	5	

Note:

- (1) The data are obtained from a comprehensive evaluation and are not tested in production.
- (2) When the analog peripherals such as ADC, HSECLK, HSICLK and LSICLK are turned on, extra power consideration needs to be considered.

Table 34 Power Consumption in Run Mode When the Program is Executed in Flash⁽¹⁾

Working mode	Condition	-40°C		25°C		105°C		125°C		Unit
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	
HSECLK16, enabling all peripherals ⁽²⁾	f _{HCLK} =64MHz	8.40	11	8.30	11	8.32	11	8.49	11	mA
HSECLK16, disabling all peripherals	f _{HCLK} =64MHz	5.70	8	4.99	8	5.01	8	5.13	8	
HSICLK, enabling all peripherals ⁽²⁾	f _{HCLK} =64MHz	6.38	10	6.49	10	6.68	10	6.82	10	
HSICLK, disabling all peripherals	f _{HCLK} =64MHz	3.57	7	3.64	7	3.80	7	3.96	7	

Note:

- (1) The data are obtained from a comprehensive evaluation and are not tested in production. Power consumption is based on measured results for reference only.
- (2) When the analog peripherals such as ADC, HSECLK, HSICLK and LSICLK are turned on, extra power consideration needs to be considered.

Table 35 Power Consumption in Run Mode When the Program is Executed in RAM⁽¹⁾

Working mode	Condition	-40°C		25°C		105°C		125°C		Unit
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	
HSECLK16, enabling all peripherals ⁽²⁾	f _{HCLK} =64MHz	8.20	11	8.22	11	8.26	11	8.39	11	mA
HSECLK16, disabling all peripherals	f _{HCLK} =64MHz	5.50	8	5.52	8	5.54	8	5.67	8	
HSICLK, enabling all peripherals ⁽²⁾	f _{HCLK} =64MHz	7.48	10	7.57	10	7.74	10	7.87	10	
HSICLK, disabling all peripherals	f _{HCLK} =64MHz	4.84	7	4.90	7	5.05	7	5.17	7	

Note:

- (1) The data are obtained from a comprehensive evaluation and are not tested in production. Power consumption is based on measured results for reference only.
- (2) When the analog peripherals such as ADC, HSECLK, HSICLK and LSICLK are turned on, extra power consideration needs to be considered.

5.8 Wake-up time in low power consumption mode

Low power consumption wake-up time is measured from the start of the wake-up event until the user program reads the first instruction, where $V_{DD}=V_{DDA}$.

Table 36 Low power consumption wake-up time⁽¹⁾

Symbol	Parameter	Condition	Typical value ($T_A=25^{\circ}\text{C}$)	Maximum value	Unit
t_{WUSTOP}	Wake up from stop mode	-	42	-	μs
$t_{WUSTANDBY}$	Wake up from standby mode	-	170	-	
$t_{WUSLEEP}$	Wake up from sleep mode	-	1.5	-	

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.9 I/O port characteristics

Table 37 DC Characteristics ($T_A=-40^{\circ}\text{C}-125^{\circ}\text{C}$, $V_{DD}=2.75\sim 4\text{V}$)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{IL}	Input low level voltage	All I/O pins	-	-	$0.3V_{DD}$	V
V_{IH}	Input high level voltage	All I/O pins	$0.7V_{DD}$	-	-	
V_{hys}	Schmitt trigger hysteresis	STDA I/O	$0.1V_{DD}$	-	-	
V_{OL}	IO output low level voltage	$I_{OL}=3\text{mA}$	-	-	0.5	
V_{OH}	IO output high level voltage	$I_{OH}=3\text{mA}$	$V_{DD}-0.4$	-	-	
V_{OL}	IO output low level voltage	$I_{OL}=12\text{mA}$	-	-	1.5	
V_{OH}	IO output high level voltage	$I_{OH}=12\text{mA}$	$V_{DD}-1.3$	-	-	
I_{OL}	IO output low current	$V_{OL}=0.4$	3	-	-	mA
I_{OH}	IO output high current	$V_{DD}-V_{OH}=0.4$	3	-	-	
I_{OL}	IO output low current	$V_{OL}=1.3$	12	-	-	
I_{OH}	IO output high current	$V_{DD}-V_{OH}=1.3$	12	-	-	
I_{OLA}	I_{OL} total current	-	-	100	-	
I_{OHA}	I_{OH} total current	-	-	100	-	
I_{lkg}	Input leakage current	STD I/O $V_{DD}\leq V_{IN}\leq 5\text{V}$	-	-	1.5	μA
R_{PU}	Weak pull-up equivalent resistance	$V_{IN}=V_{SS}$	25	40	55	$\text{k}\Omega$
R_{PD}	Weak pull-down equivalent resistance	$V_{IN}=V_{DD}$	25	40	55	

Table 38 DC Characteristics ($T_A=-40^{\circ}\text{C}\sim 125^{\circ}\text{C}$, $V_{DD}=4\sim 5.5\text{V}$)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V_{IL}	Input low level voltage	All I/O pins	-	-	$0.3V_{DD}$	V
V_{IH}	Input high level voltage	All I/O pins	$0.7V_{DD}$	-	-	
V_{hys}	Schmitt trigger hysteresis	STDA I/O	$0.1V_{DD}$	-	-	
V_{OL}	IO output low level voltage	$I_{OL}=5\text{mA}$	-	-	0.5	
V_{OH}	IO output high level voltage	$I_{OL}=5\text{mA}$	$V_{DD}-0.4$	-	-	
V_{OL}	IO output low level voltage	$I_{OL}=20\text{mA}$	-	-	1.5	
V_{OH}	IO output high level voltage	$I_{OL}=20\text{mA}$	$V_{DD}-1.3$	-	-	
I_{OL}	IO output low current	$V_{OL}=0.4$	5	-	-	mA
I_{OH}	IO output high current	$V_{DD}-V_{OH}=0.4$	5	-	-	
I_{OL}	IO output low current	$V_{OL}=1.3$	20	-	-	
I_{OH}	IO output high current	$V_{DD}-V_{OH}=1.3$	20	-	-	
I_{OLA}	I_{OL} total current	-	-	100	-	
I_{OHA}	I_{OH} total current	-	-	100	-	
I_{lkg}	Input leakage current	STD I/O $V_{DD}\leq V_{IN}\leq 5\text{V}$	-	-	1.5	μA
R_{PU}	Weak pull-up equivalent resistance	$V_{IN}=V_{SS}$	25	40	55	$k\Omega$
R_{PD}	Weak pull-down equivalent resistance	$V_{IN}=V_{DD}$	25	40	55	

Table 39 Filter Characteristics

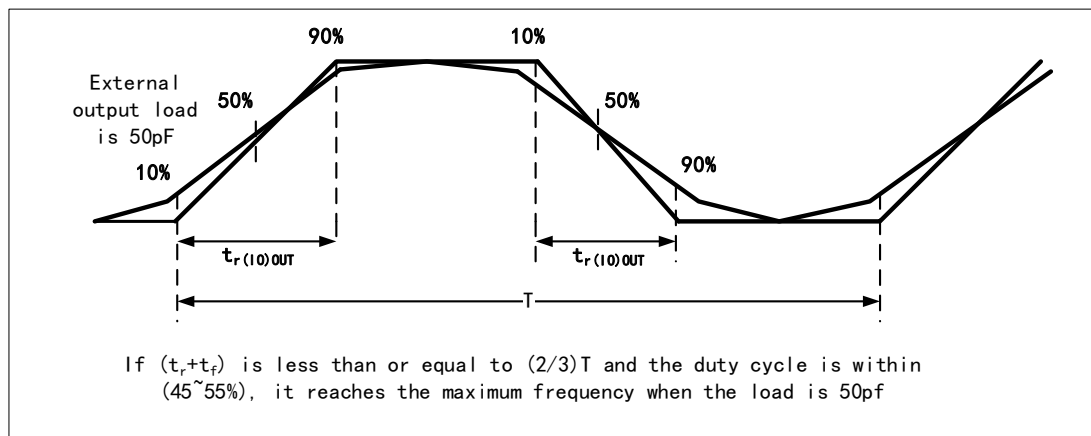
FILTER_ENY	Parameter	Condition	Typical value	Maximum value	Unit
1	Rising edge	$T_A=-40^{\circ}\text{C}\sim 125^{\circ}\text{C}$, $V_{DD}=2.75\sim 5.5\text{V}$	84	178	ns
	Falling edge		67	119	

Table 40 AC Characteristics ($T_A=25^{\circ}\text{C}$)

OSSELy[1:0]	Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
00(2MHz)	$f_{\max(\text{IO})\text{out}}$	Maximum frequency	$C_L=50\text{pF}$, $V_{DD}=2.75\sim 5.5\text{V}$	-	2	MHz
	$t_{\text{r}(\text{IO})\text{out}}$	Output high to low level fall time		-	120	ns
	$t_{\text{r}(\text{IO})\text{out}}$	Output low to high rise time		-	120	
01(10MHz)	$f_{\max(\text{IO})\text{out}}$	Maximum frequency	$C_L=50\text{pF}$, $V_{DD}=2.75\sim 5.5\text{V}$	-	10	MHz

OSSELY[1:0]	Symbol	Parameter	Condition	Minimum value	Maximum value	Unit	
	$t_{r(I/O)out}$	Output high to low level fall time		-	25	ns	
	$t_{r(I/O)out}$	Output low to high rise time		-	25		
10(20MHz)	$f_{max(I/O)out}$	Maximum frequency	$C_L=30pF,$ $V_{DD}=2.75\sim 5.5V$	-	20	MHz	
	$t_{r(I/O)out}$	Output high to low level fall time		-	10		ns
	$t_{r(I/O)out}$	Output low to high rise time		-	10		
11(40MHz)	$f_{max(I/O)out}$	Maximum frequency	$C_L=30pF,$ $V_{DD}=2.75\sim 5.5V$	-	40	MHz	
	$t_{r(I/O)out}$	Output high to low level fall time		-	8		ns
	$t_{r(I/O)out}$	Output low to high rise time		-	8		

Figure 10 Input/Output AC Characteristics Definitions



5.10 NRST pin characteristics

The NRST pin input driver uses a CMOS process which connects a permanent pull-up resistor R_{PU} .

Table 41 NRST Pin Characteristics ($T_A=-40\sim 125^\circ C, V_{DD}=2.75\sim 5.5V$)

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
$V_{IL(NRST)}$	NRST input low voltage	-	-	-	$0.3V_{DD}$	V
$V_{IH(NRST)}$	NRST input high voltage	-	$0.7V_{DD}$	-	-	
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	-	$0.1V_{DD}$	-	-	

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
R _{PU}	Weak pull-up equivalent resistance	V _{IN} =V _{SS}	25	40	55	kΩ
WFRST	NRST input filter pulse	-	-	50	240	ns
R _{EXT_PU}	External pull-up resistor	-	1	10	-	kΩ
C _{EXT}	External capacitor	-	-	100	500	nF

5.11 Communication interface

5.11.1 SPI interface characteristics

Table 42 SPI Characteristics (T_A=25°C, V_{DD}=5V)⁽¹⁾

Symbol	Parameter	Condition	Minimum value	Maximum value	Unit
f _{SCK} 1/t _{c(SCK)}	SPI clock frequency	Master mode	-	16	MHz
		Slave mode	-	16	
t _{r(SCK)} t _{f(SCK)}	SPI clock rise and fall time	Load capacitance: C=15pF	-	8	ns
t _{su(NSS)}	NSS setup time	Slave mode	110	-	ns
t _{h(NSS)}	NSS hold time	Slave mode	56.67	-	ns
t _{w(SCKH)} t _{w(SCKL)}	SCK high and low level time	Master mode, f _{PCLK} =64MHz, Prescaler factor=8	54	57	ns
t _{su(MI)} t _{su(SI)}	Data input setup time	Master mode	12	-	ns
		Slave mode	20	-	
t _{h(MI)} t _{h(SI)}	Data input hold time	Master mode	34	-	ns
		Slave mode	22	-	
t _{a(SO)}	Data output access time	Slave mode, f _{PCLK} =20MHz	-	40	ns
t _{dis(SO)}	Disable time of data output	Slave mode	-	45	ns
t _{v(SO)}	Effective time of data output	Slave mode (after enabling the edge)	-	50	ns
t _{v(MO)}	Effective time of data output	Master mode (after enabling the edge)	-	6	ns
t _{h(SO)}	Data output hold time	Slave mode (after enabling the edge)	11.5	-	ns
t _{h(MO)}		Master mode (after enabling the edge)	2	-	

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

Figure 11 SPI Timing Diagram – Slave Mode and CPHA=0

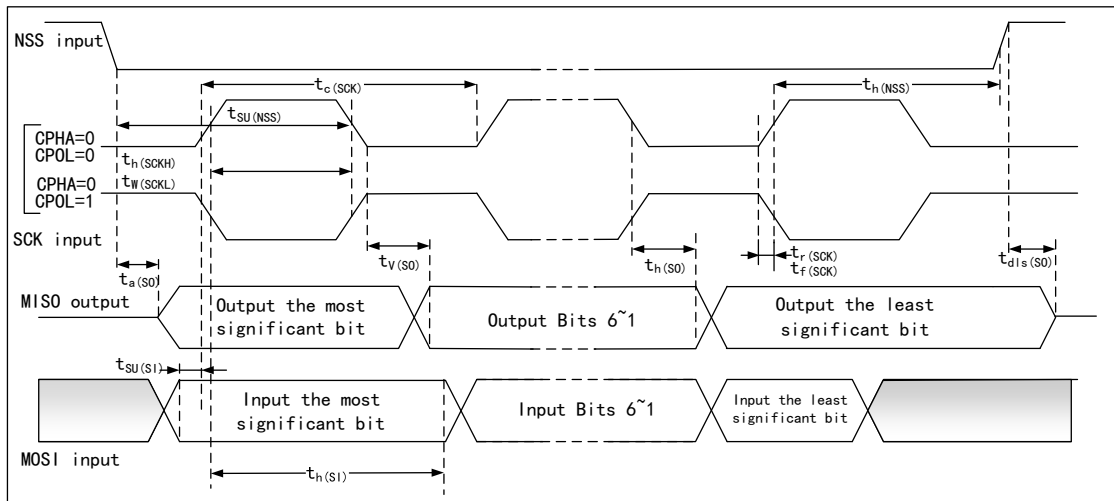
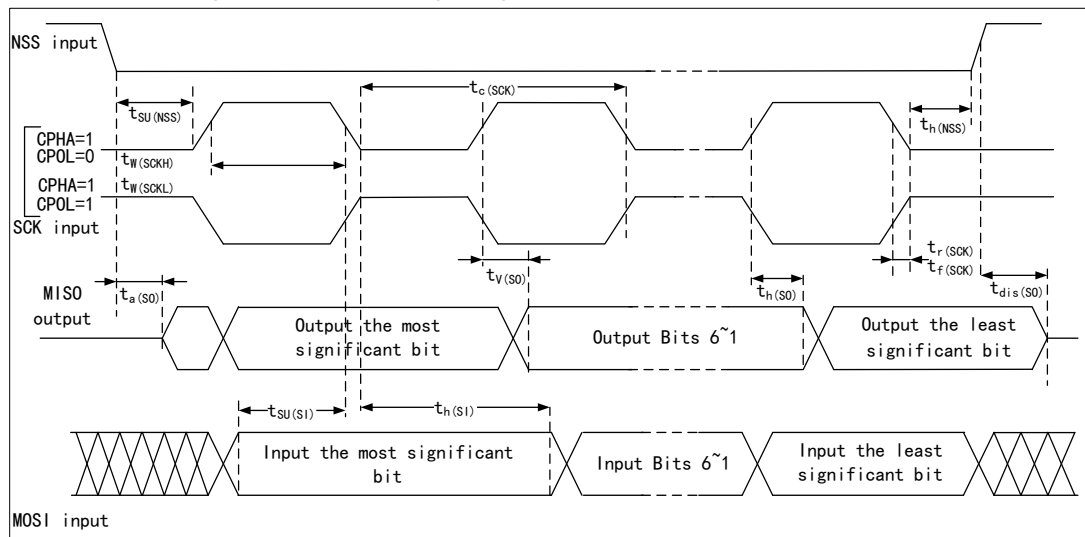
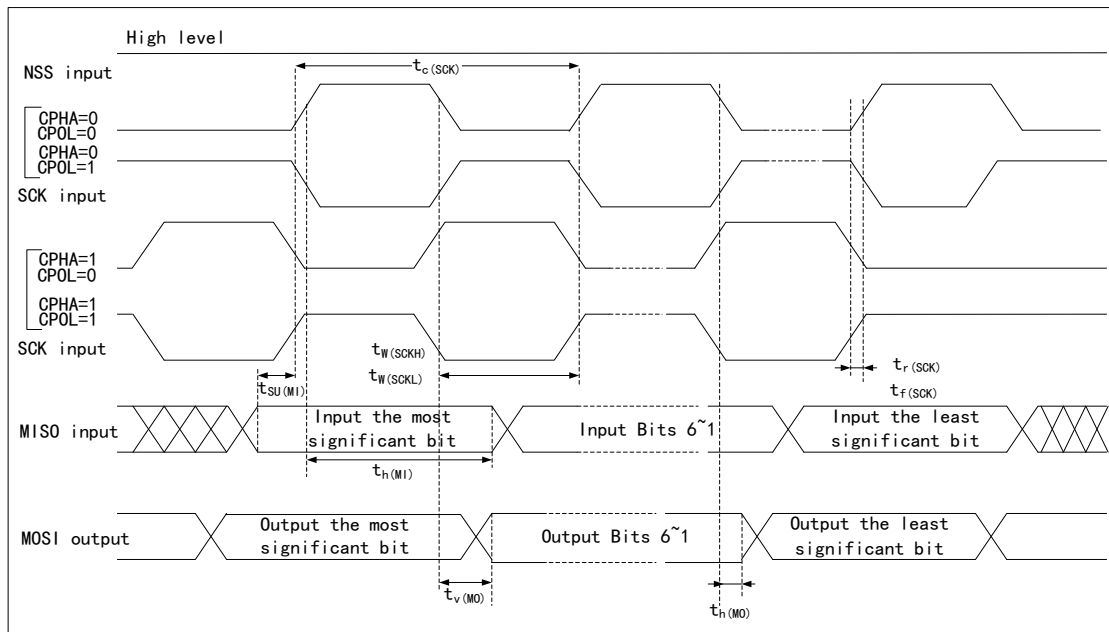


Figure 12 SPI Timing Diagram – Slave Mode and CPHA=1



Note: The measuring points are set at CMOS levels: 0.3V_{DD} and 0.7V_{DD}.

Figure 13 SPI Timing Diagram – Master Mode



Note: The measuring points are set at CMOS levels: 0.3V_{DD} and 0.7V_{DD}.

5.12 ADC

5.12.1 Built-in reference voltage characteristics

Table 43 Built-in Reference Voltage Characteristics ⁽¹⁾

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
T _{S_vrefint}	When reading the internal reference voltage, sampling time of ADC	-	4	-	-	μs
ΔV _{REFINT}	Built-in reference voltage extended to temperature range	-	-25	-	25	mV

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.12.2 12-bit ADC characteristics

Table 44 12-bit ADC Characteristics ⁽¹⁾

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
V _{DDA}	Supply voltage	-	2.75	-	5.5	V
I _{DDA}	ADC power consumption	f _{ADC} =14MHz, sampling time = 1.5 f _{ADC}	-	1	-	mA
f _{ADC}	ADC frequency	-	0.6	-	14	MHz

Symbol	Parameter	Condition	Minimum value	Typical value	Maximum value	Unit
C _{ADC}	Internal sampling and holding capacitance	-	-	5	-	pF
R _{ADC}	Sampling resistor	-	-	-	1000	Ω
t _s	Sampling time	f _{ADC} =14MHz	0.107	-	17.1	μs
T _{CONV}	Sampling and conversion time	f _{ADC} =14MHz, 12-bit conversion	1	-	18	
f _{CONV}	ADC conversion frequency	f _{ADC} =14MHz	0.056	0.206	1	Msp/s

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

Table 45 12-bit ADC Accuracy⁽¹⁾

Symbol	Parameter	Condition	Typical value	Maximum value	Unit
E _T	Total error	f _{PCLK} =64MHz, f _{ADC} =14MHz, V _{DDA} =2.75V-5.5V T _A =-40°C~125°C	±6	-	LSB
E _O	Offset error		±5	-	
E _G	Gain error		±1	-	
E _D	Differential linear error		±1	-	
E _L	Integral linear error		±1.9	-	

Note: (1) The data are obtained from a comprehensive evaluation and are not tested in production.

5.12.3 Temperature sensor characteristics

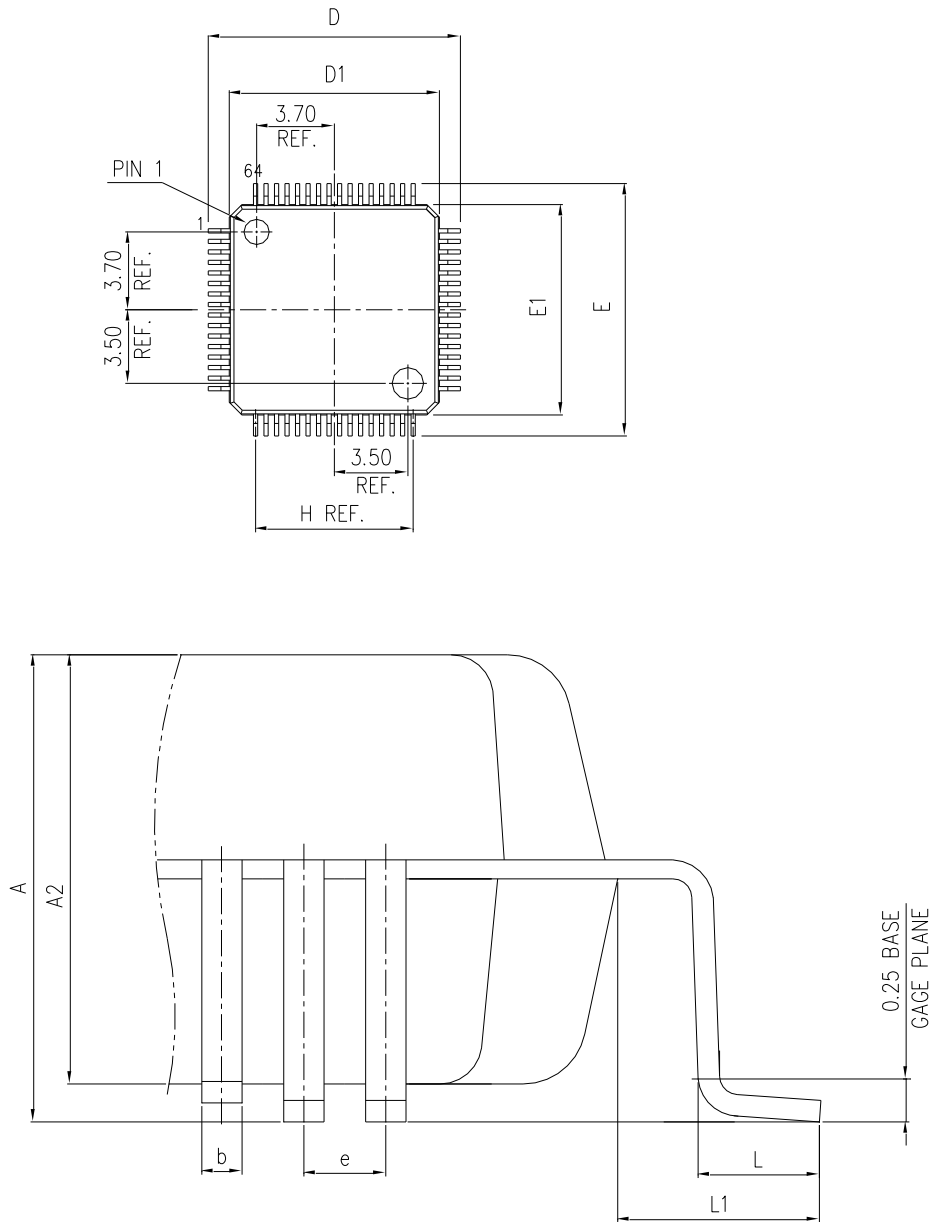
Table 46 Temperature Sensor Characteristics

Symbol	Parameter	Minimum value	Typical value	Maximum value	Unit
TSENSOR	Temperature Sensor Error	-	±1	±5	°C
Avg_Slope	Average slope	3.7	3.9	4.1	mV/°C
V30	Reference voltage at 25°C(±5°C)	1.34	1.43	1.52	V
	Reference voltage at 125°C(±5°C)	0.9	-	1.34	
	Reference voltage at -40°C(±5°C)	1.52	-	1.75	
ts_temp	ADC sampling temperature time	4	-	17.1	μs

6 Package Information

6.1 LQFP64 package information

Figure 14 LQFP64 Package Diagram



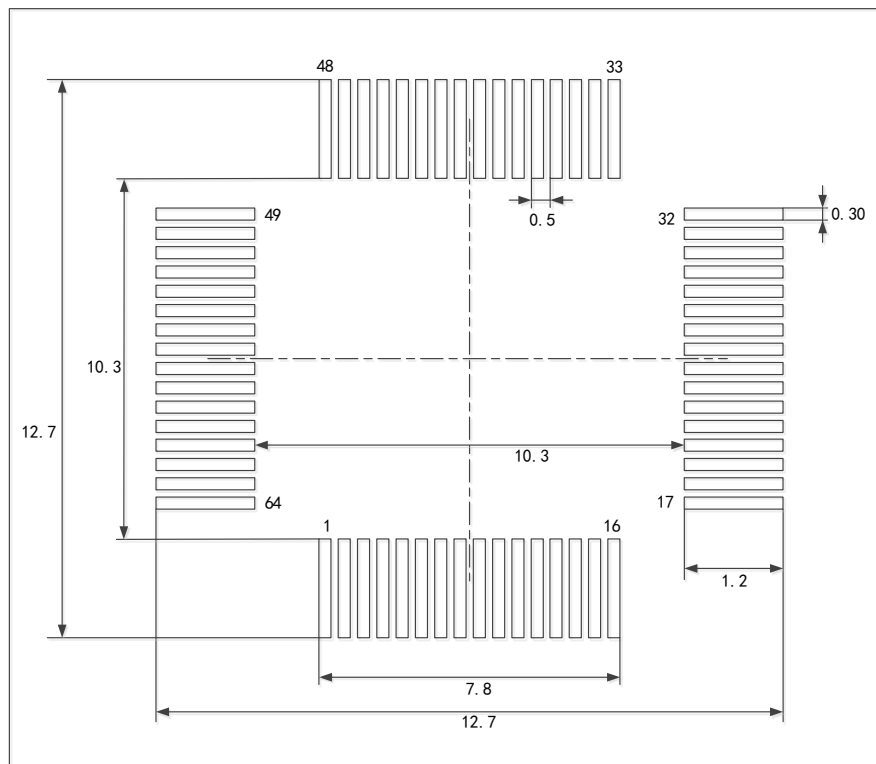
- (1) The figure is not drawn to scale.
- (2) All pins should be soldered to the PCB.

Table 47 LQFP64 Package Data

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX.1.600	OVERALLHEIGHT
2	A2	1.400±0.050	PKGTHICKNESS
3	D	12.000±0.200	LEADTIPTOTIP
4	D1	10.000±0.100	PKGLENGTH
5	E	12.000±0.200	LEADTIPTOTIP
6	E1	10.000±0.100	PKGWIDTH
7	L	0.600±0.150	FOOTLENGTH
8	L1	1.000REF	LEADLENGTH
9	e	0.500BSC	LEADPITCH
10	b	0.220±0.050	LEADWIDTH

Note: Dimensions are marked in millimeters.

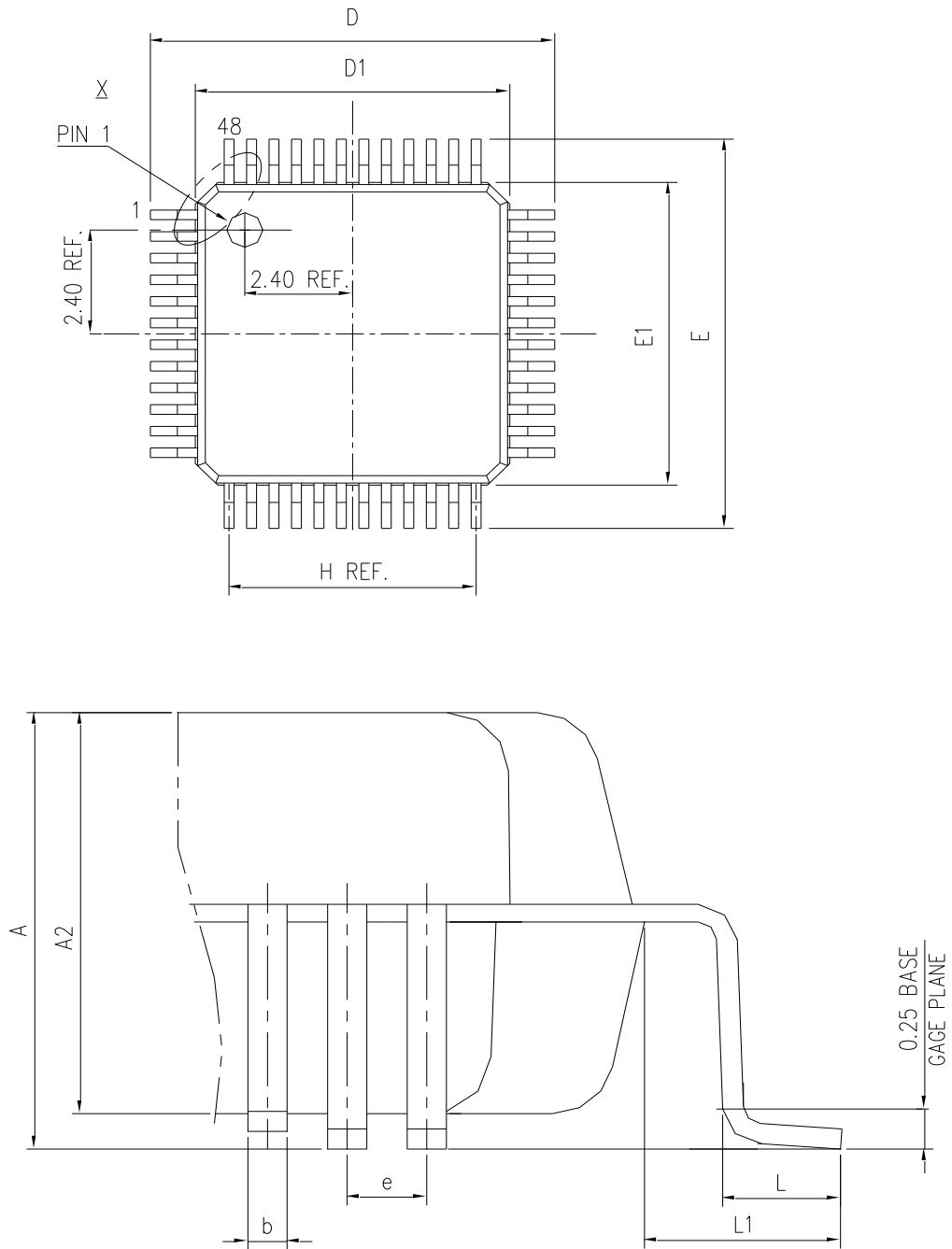
Figure 15 LQFP64 Welding Layout Recommendations



Note: Dimensions are marked in millimeters.

6.2 LQFP48 package information

Figure 16 LQFP48 Package Diagram



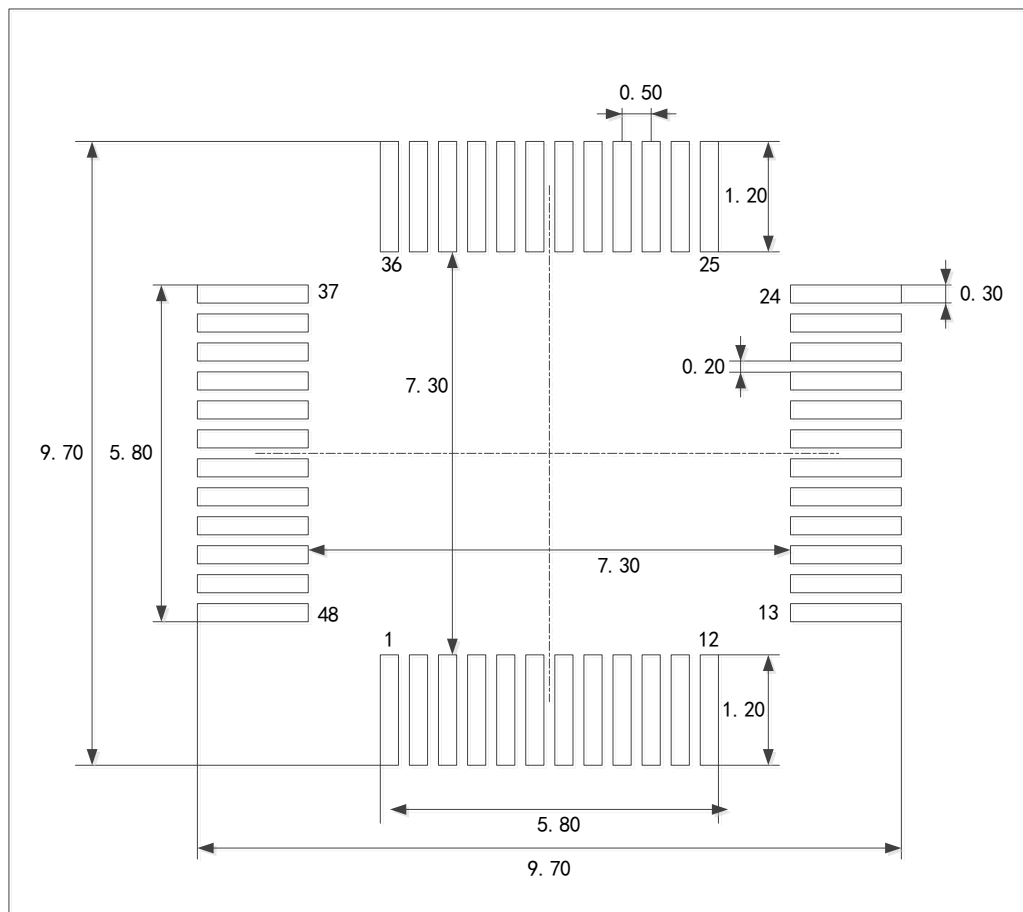
Note: The figure is not drawn to scale.

Table 48 LQFP48 Package Data

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX.1.60	OVERALLHEIGHT
2	A2	1.40±0.05	PKGTHICKNESS
3	D	9.00±0.20	LEADTIPTOTIP
4	D1	7.00±0.10	PKGLENGTH
5	E	9.00±0.20	LEADTIPTOTIP
6	E1	7.00±0.10	PKGWIDTH
7	L	0.60±0.15	FOOTLENGTH
8	L1	1.00REF	LEADLENGTH
9	e	0.50BSC	LEADPITCH
10	b	0.22±0.050	LEADWIDTH

Note: Dimensions are marked in millimeters.

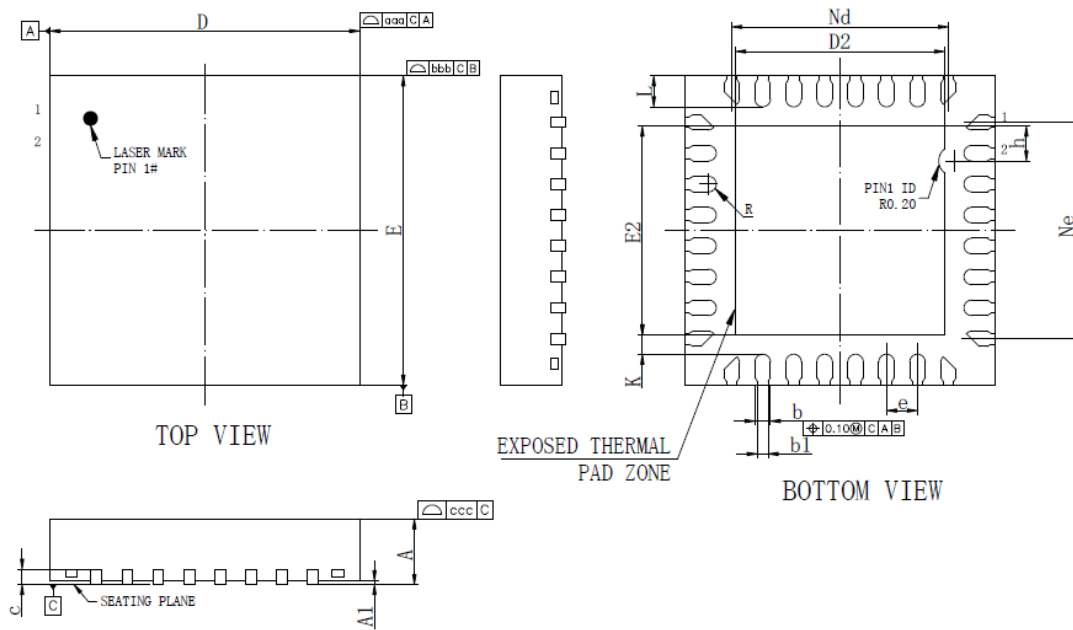
Figure 17 LQFP48 Welding Layout Recommendations



Note: Dimensions are marked in millimeters.

6.3 QFN32 package information

Figure 18 QFN32 (4mm x 4mm) Package Diagram



Note: The figure is not drawn to scale.

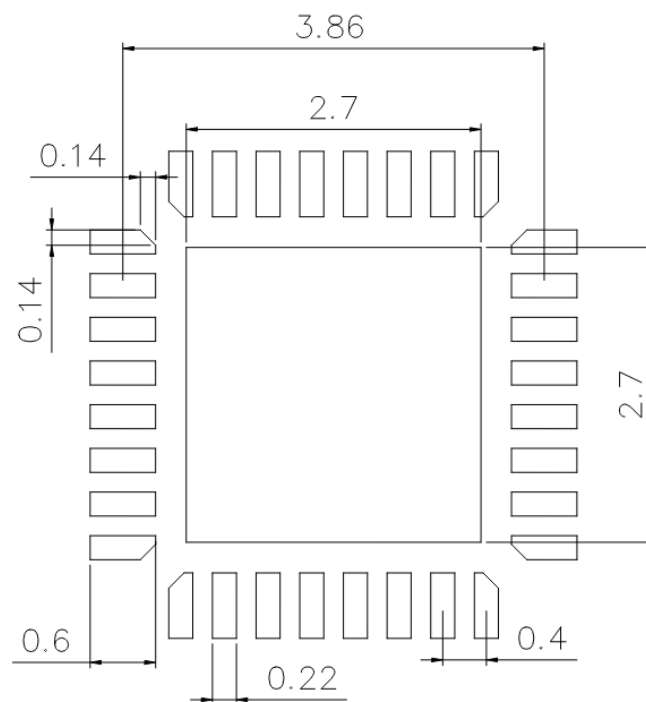
Table 49 QFN32 (4mm x 4mm) Package Data

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
b	0.15	0.20	0.25
b1	0.14REF		
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.65	2.70	2.75
e	0.40BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.65	2.70	2.75
Ne	2.80BSC		
K	0.25REF		
L	0.35	0.40	0.45

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
h	0.40	0.45	0.50
R	0.08	0.10	0.15
aaa	0.10		
bbb	0.10		
ccc	0.05		

Note: Dimensions are marked in millimeters.

Figure 19 QFN32 (4mm x 4mm) Welding Layout Recommendations



Note: Dimensions are marked in millimeters.

6.4 Package identification

The LQFP package identification is listed below:

Figure 20 LQFP Package Identification

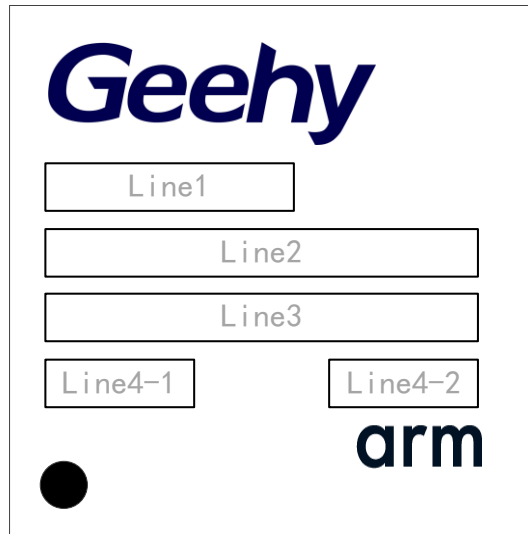


Table 50 LQFP Silkscreen Descriptions

Symbol	Descriptions
Geehy	Company Name
Line1	Device Family
Line2	Product Model
Line3	Batch Number
Line4-1	Internal Traceable Code
Line4-2	Year and Week Number
arm	Arm Authorized Trademark
●	PIN1 Location

Note: The length of each line may vary and is not fixed.

The package identification of QFN32 is listed below:

Figure 21 QFN32 Package Identification

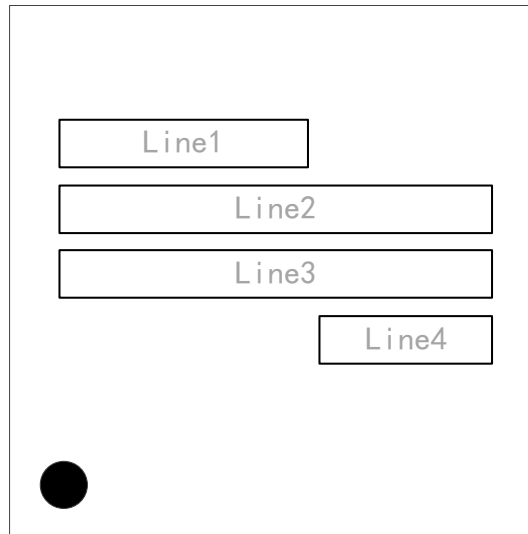



Table 51 QFN32 Silkscreen Descriptions

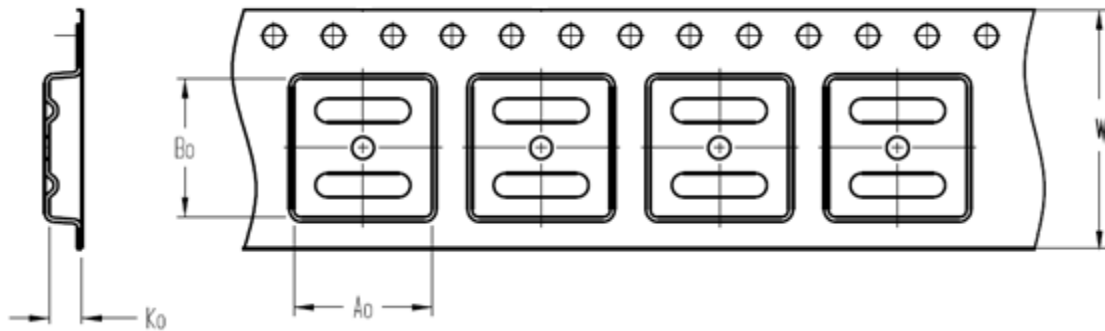
Symbol	Descriptions
Line1	Product Model
Line2	Batch Number
Line3	Internal Traceable Code
Line4	Year and Week Number
	PIN1 Location

Note: The length of each line may vary and is not fixed.

7 Packaging Information

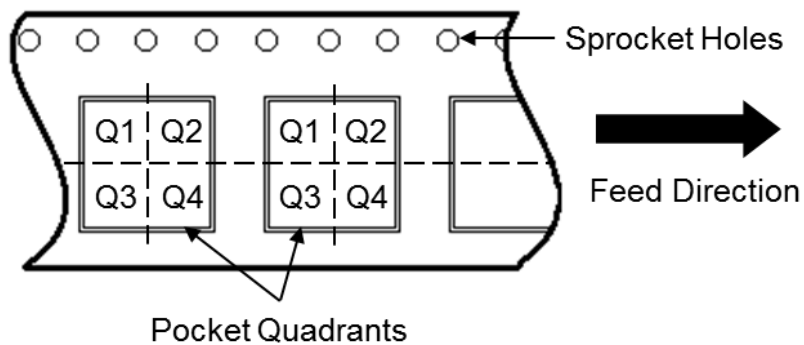
7.1 Reel packaging

Figure 22 Reel Packaging Specification Drawing



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape

Quadrant Assignments for PIN1 Orientation in Tape



Reel Dimensions:

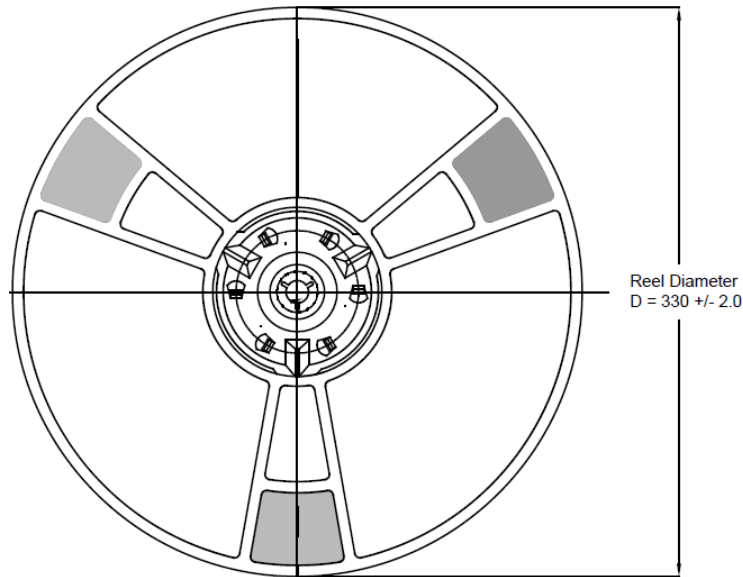


Table 52 Reel Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	ReelDiameter (mm)	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	Pin1 Quadrant
G32A1085MAT0MLH	LQFP	64	1500	330	12.35	12.35	2.2	24	Q1
G32A1085MAT0MLF	LQFP	48	2000	330	9.3	9.3	2.2	16	Q1
G32A1085MAT0MFM	QFN	32	5000	330	4.3	4.3	1.1	12	Q1
G32A1065MAT0MLH	LQFP	64	1500	330	12.35	12.35	2.2	24	Q1
G32A1065MAT0MLF	LQFP	48	2000	330	9.3	9.3	2.2	16	Q1
G32A1065MAT0MFM	QFN	32	5000	330	4.3	4.3	1.1	12	Q1
G32A1045MAT0MLF	LQFP	48	2000	330	9.3	9.3	2.2	16	Q1
G32A1045MAT0MFM	QFN	32	5000	330	4.3	4.3	1.1	12	Q1

7.2 Tray packaging

Figure 23 Tray Packaging Diagram

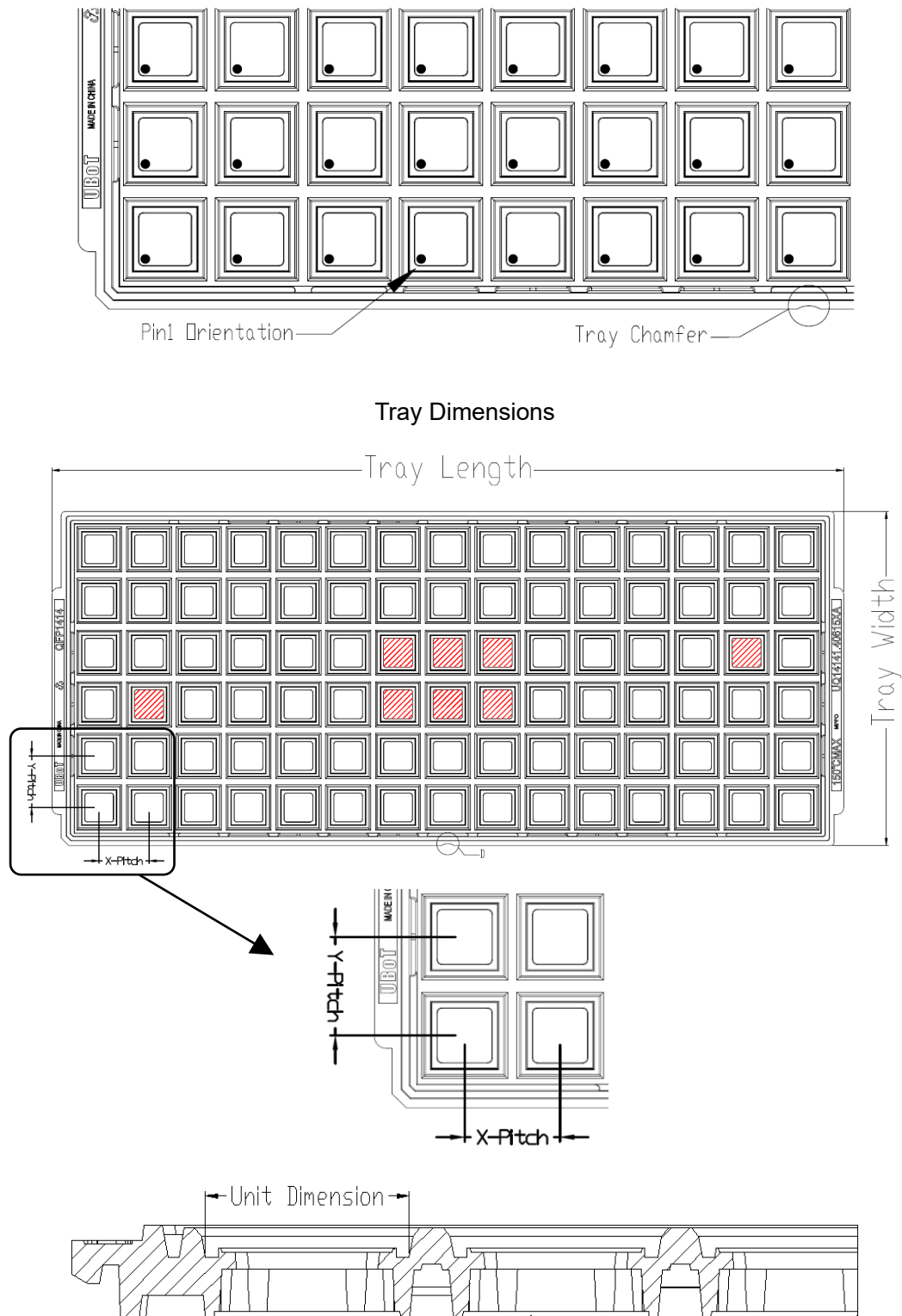


Table 53 Tray Packaging Parameter Specification Table

Device	Package Type	Pins	SPQ	X-Dimension (mm)	Y-Dimension (mm)	X-Pitch (mm)	Y-Pitch (mm)	Tray Length (mm)	Tray Width (mm)
G32A1085MAT0MLH	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
G32A1085MAT0MLF	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
G32A1085MAT0MFM	QFN	32	4900	4.2	4.2	8.8	9.2	322.6	135.9
G32A1065MAT0MLH	LQFP	64	1600	12.3	12.3	15.2	15.7	322.6	135.9
G32A1065MAT0MLF	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
G32A1065MAT0MFM	QFN	32	4900	4.2	4.2	8.8	9.2	322.6	135.9
G32A1045MAT0MLF	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9
G32A1045MAT0MFM	QFN	32	4900	4.2	4.2	8.8	9.2	322.6	135.9

8 Ordering Information

Table 54 Product Naming Definitions

Product Name			
G32A1085MAT0MLH			
Naming example	Definition	Naming	Description
G32	Product family	G32	32-bit microcontroller
A	Product type	A	Automotive
1	Product sub-type	1	General MCU
0	Core	0	Arm® Cortex®-M0+
8	Flash size	8	256KB
		6	128KB
		4	64KB
5	Product number	5	Product number
M	Frequency	M	64MHz
A	Reserved	A	-
T0	Internal version	T0	Internal version
M	Temperature	V	105°C
		M	125°C
LH	Package type	LH	LQFP64
		LF	LQFP48
		FM	QFN32

Table 55 Ordering Information Table

Order Code	FLASH(KB)	SRAM(KB)	SPQ	Package	Packaging	Temperature range
G32A1085MAT0MLH	256KB+32KB	32KB	1500	LQFP64	Reel	-40°C~125°C
G32A1085MAT0MLF	256KB+32KB	32KB	2000	LQFP48	Reel	-40°C~125°C
G32A1085MAT0MFM	256KB+32KB	32KB	5000	QFN32	Reel	-40°C~125°C
G32A1085MAT0MLH	256KB+32KB	32KB	1600	LQFP64	Tray	-40°C~125°C
G32A1085MAT0MLF	256KB+32KB	32KB	2500	LQFP48	Tray	-40°C~125°C
G32A1085MAT0MFM	256KB+32KB	32KB	4900	QFN32	Tray	-40°C~125°C

Order Code	FLASH(KB)	SRAM(KB)	SPQ	Package	Packaging	Temperature range
G32A1065MAT0MLH	128KB+32KB	16KB	1500	LQFP64	Reel	-40°C~125°C
G32A1065MAT0MLF	128KB+32KB	16KB	2000	LQFP48	Reel	-40°C~125°C
G32A1065MAT0MFM	128KB+32KB	16KB	5000	QFN32	Reel	-40°C~125°C
G32A1065MAT0MLH	128KB+32KB	16KB	1600	LQFP64	Tray	-40°C~125°C
G32A1065MAT0MLF	128KB+32KB	16KB	2500	LQFP48	Tray	-40°C~125°C
G32A1065MAT0MFM	128KB+32KB	16KB	4900	QFN32	Tray	-40°C~125°C
G32A1045MAT0MLF	64KB+16KB	8KB	2000	LQFP48	Reel	-40°C~125°C
G32A1045MAT0MFM	64KB+16KB	8KB	5000	QFN32	Reel	-40°C~125°C
G32A1045MAT0MLF	64KB+16KB	8KB	2500	LQFP48	Tray	-40°C~125°C
G32A1045MAT0MFM	64KB+16KB	8KB	4900	QFN32	Tray	-40°C~125°C

Note: SPQ is the smallest packaging quantity.

9 Commonly Used Modules

Table 56 Commonly Used Modules

Full name	Abbreviation
Reset management unit	RMU
Clock management unit	CMU
Reset and clock management	RCM
External Interrupt	EINT
General-purpose IO	GPIO
Multiplexing IO	AFIO
Wake-up controller	WUPT
Buzzer	BUZZER
Independent watchdog timer	IWDT
Timer	TMR
CRC controller	CRC
Power Management Unit	PMU
DMA controller	DMA
Analog-to-digital converter	ADC
Real-time clock	RTC
External memory controller	EMMC
Controller area network	CAN
Controller area network flexible data	CAN FD
Serial peripheral interface	SPI
Universal asynchronous transmitter receiver	UART
Universal synchronous and asynchronous transmitter receiver	USART
Flash interface control unit	FMC
Advanced encryption module	AES
True random number generator	TRNG
Cryptographic Hash function	SHA256

10 Revision History

Table 57 Document Revision History

Date	Version	Revision History
February 2026	1.0	<ul style="list-style-type: none"> • Initial release
April 2026	1.1	<ul style="list-style-type: none"> • Updated electrical characteristics data based on test results. • Added QFN32 (4mm x 4mm) recommended welding layout.
May 2026	1.2	<ul style="list-style-type: none"> • Modified the average slope of the temperature sensor and the maximum voltage at -40°C. • Modified the minimum operating voltage from 2.7V to 2.75V. • Modified the maximum value of the PDR threshold.

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